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GaAs MMIC mixer for 8-12GHz, based on 0.5 μm gate length D-MESFETS. Volume 1: Design and layout.

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ABSTRACT

A description is given of the design of an 8-12 GHz GaAs MMIC (Monolithic Microwave Integrated Circuit) mixer. The mixer consists of a dual-FET mixing element, active input and output matching and bias networks. The mixer is designed with the TriQuint HA-process, which uses 0.5μm gate length depletion mode MESFET devices.
The design goals are a return loss better than -15dB for the inputs and output and a conversion gain better than 0dB.
The complete circuit is biased with a symmetrical power supply of ±5 volts and has autobiasing through on-chip bias networks. The total power consumption of the circuit is 350mW. The dimensions of the chip are 1.4x1.4mm.
This report is part one of two reports and gives an in-depth description of the circuit design. Simulation results and chip layout are provided. A second report will give the measurement results as well as an evaluation of them.

rapport no. : FEL-89-B277
titel : GaAs MMIC mixer voor 8-12GHz, gerealiseerd met 0,5 μm gate lengte D-MESFETS. Deel 1: Ontwerp en layout

auteur(s) : ing. T.C.B. Tieman, ing. R. Grooters
instituut : Fysisch en Elektronisch Laboratorium TNO

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SAMENVATTING

Het ontwerp van een 8-12 GHz GaAs MMIC (Monolithic Microwave Integrated Circuit) mixer wordt beschreven.
De mixer heeft een dual-FET mengelement, aktieve in-en uitgangs aanpassing en een voedingsnetwerk. De mixer is gerealiseerd met het Triquint HA-proces, dat depletie MESFETs oplevert met een gate-lengte van 0,5 μm.
De specificaties waarnaar gestreefd wordt zijn in- en uitgang reflekties van kleiner dan -15 dB en een konversie verlies van 0dB.
Het gehele circuit wordt gevoed met een symmetische voedingsspanning van +5 en -5 volt en alle benodigde spanningen worden met speciale netwerken op de chip gerealiseerd. Het totale vermogensverbruik is 350 mW. De afmetingen van de chip zijn 1,4 * 1.4 mm.
Dit rapport is deel 1 van twee rapporten en geeft een volledig beeld van het ontwerp van de mixer. Simulatie resultaten en de layout worden beschreven. Een tweede rapport zal de meetresultaten en een evaluatie bevatten.

1. INTRODUCTION.

The Physics and Electronics Laboratory TNO has a lot of experience in designing and fabricating thin film microwave integrated circuits. The next step in miniaturizing circuits is to integrate all components on one chip: Monolithic Microwave Integrated Circuit, MMIC.
These circuits have certain advantages over MIC designs:

- reduced part count.
- higher circuit reliability, due to less man-made interconnections.
- potential lower cost for large quantities.
- integration of functions in one single-chip.

Most applications will be for the military market, for instance active phased array radar, smart munition and fast signal processing. Also satellite systems and communication systems will benefit from the advantages.

This report describes the design of an 8-12GHz GaAs MMIC mixer which is part of a project with a wide scope. The project's aim is to get a deeper understanding in the design of MMICs on GaAs. This has to be achieved through the following means:

- designing two or three different circuits
- realize them at different factories
- setting up a measurement tool for the chips

The mixer design was done as part of a course offered by TriQuint [1]. Included in the course was the design and production of 15 dies. The process used by TriQuint for the course is the HA-process which is based on 0.5μm gate lenght depletion mode MESFET devices.
A mixer design was chosen because mixers weren't commercially available at that time. Many other circuits, like switches and amplifiers, were.

The mixer consists of a mixing-part built with two FETs, an active input matching for the LO and RF and an active matching for the IF output. The mixer is autobiasing through on chip bias networks and is fed from a symmetrical power supply. Applications for this kind of mixer are in the receiving unit of many radar and telecommunication systems and especially in single-chip FMCW radar front-ends.
This report is part one of two reports and gives an in-depth description of the circuit design. Simulation results and chip layout are provided. The second report will give the measurement results as well as an evaluation of them.

2. THE HA PROCESS OF TRIQUINT.

The TriQuint HA process is based on a 0.5μm gate length depletion mode MESFET. With the process it is possible to fabricate D-MESFETs, diodes, implanted resistors, MIM capacitors and thin film resistors. The interconnection between different devices on a circuit is achieved through two levels of metallization, of which the second level is airbridge metal. The airbridge metal gives low parasitic capacitance per unit length due to air being the surrounding dielectric layer. The isolation between different active devices is obtained through built-in isolation of the semi-insulating GaAs substrate.
The HA-process consists of 12 mask layers:

1 N- implant
2 N+ implant
3 Thin-film resistor (NiCr)
5 Ohmic metal
7 Gate metal
8 Dielectric via
9 1-metal (first level interconnect)
10 Airbridge via
11 2-metal (airbridge interconnect)
12 Passivation via
13 Allignement keys
14 Thin-film resistor contact

The numbers of the layers are corresponding with the layer numbers at TriQuint. The skipped numbers are masks that are used by TriQuint for fabrication purposes.
Figure 2.1 shows some MMIC circuit elements and there construction on the GaAs substrate.

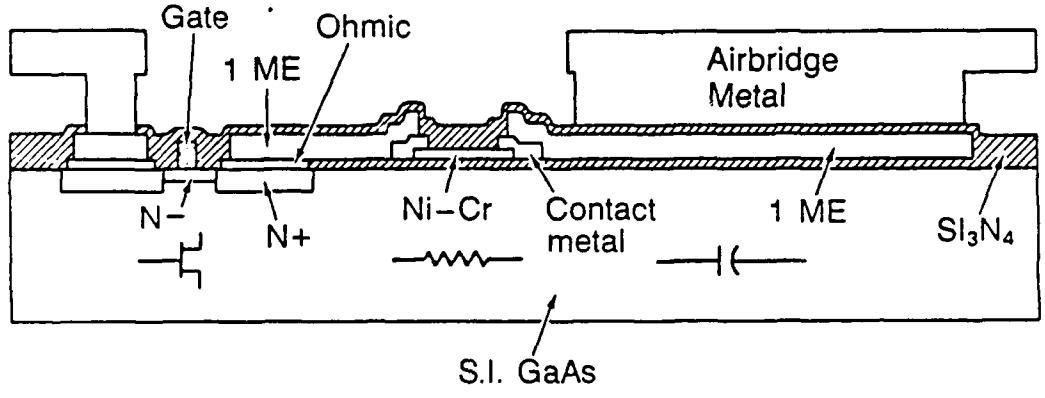


Figure 2.1 MMIC elements on GaAs.

3. THE SPECIFICATIONS OF THE GAAS MIXER.

The specifications are based on literature and a possible requirement of a FMCW radar.

Frequencies:

RF	8-12 GHz
LO	8-12 GHz
IF	.1-1.7Ghz

Return loss:

RF	<-15dB
LO	<-15dB
IF	<-15dB

Isolation:

RF-IF	as good as possible
LO-RF	as good as possible
LO-IF	as good as possible

Conversion:

RF-IF >0dB

The noise behaviour is not dealt with. Noise models for the FETs used in the process were not available.

4. INITIAL CIRCUIT DESIGN.

In this chapter the initial circuit design is discussed and an explanation of the different sub-circuits is given.

4.1 The mixing part

The first question is what kind of mixing elements can be used. Normally the diode is used, because it is cheap and easy to handle. A disadvantage is that it gives a conversion loss of 6 to 8 dB, and the input-output matching is rather poor.
By designing a MMIC, as many FETs as needed can be used, and besides, there are a few advantages by using a FET as the mixing device:

- conversion gain is possible
- better matching of input and output
- inherent isolation between signals

In this design the mixing element is a combination of two single-gate FETs. A dual-gate FET has two disadvantages.
First, it is difficult to match the "upper gate" (gate2) to a 50Ω source impedance and second, there are no good simulation models available for dual-gate FETs.

So through splitting the dual-gate FET into two joined single-gate FETs the simulation models of a single-gate FET can be used. By using a compensation network attached to the middle of the two FETs a few advantages are obtained (figure 4.1.1):

- . a better match for the "upper gate" (gate2)
- more stability

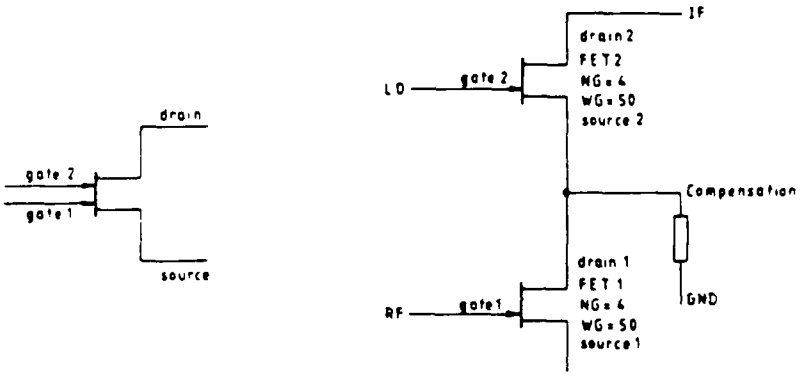


Figure 4.1.1 Use of two single-gate FETs instead of a dual-gate FET.

The RF-signal is supplied to FET1 (gate1), and the LO-signal to FET2 (gate2). The conversion products are available (IF-signal) at the drain of FET2. The dimensions of the FETs are determined by the total power, the matching and the parasitic capacitances. FETs with four gate-fingers, each with a width of 50μm, are chosen.

4.2 The matching circuits for the LO and RF inputs

There are three ways for matching the LO and RF inputs to a 50Ω source impedance:

1. The use of transmission lines. This method of design uses a large amount of chip area and for frequencies lower than 8GHz this method is not recommanded. An other disadvantage is that it is difficult to make broadband designs.
2. The use of lumped elements (resistors, inductors and capacitors). In this case the used elements are small but for broadband designs the number of elements increases as well as the used chip area.
3. The use of active matching with a FET. When looking into the source of a common-gate configuration, the RF equivalent circuit consists of a 1/gm resistance (gm=transconductance of the FET). This gm is dependent on the, free choosable, dimensions of the FET. It appears that with a gate width of 140μm (4x35μm) 1/gm is exactly 50Ω. Another advantage is that 1/gm is frequency independent.

This last method will be used to match the mixer inputs, see figure 4.2.1. There is one disadvantage and that is a mismatch loss on the drain side of the FET. This will contribute in the overal conversion gain and noise figure. To provide direct current (d.c.) bias and high frequency isolation an inductor is placed between the source and the gate.

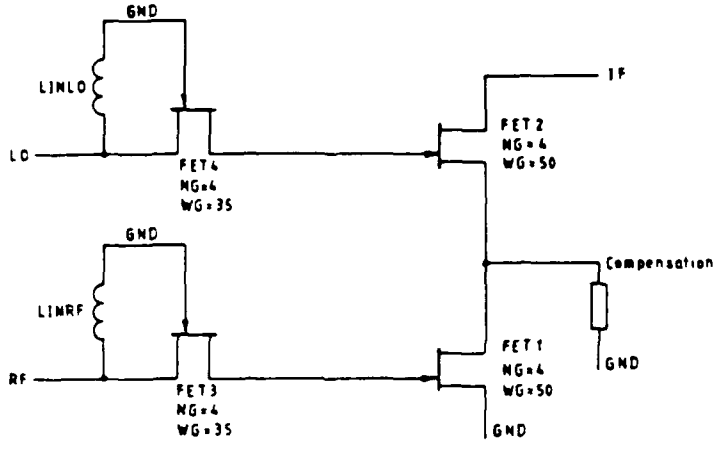


Figure 4.2.1 Active matching for the mixer inputs

4.3 The matching circuit for the IF output

The only simple solution to realize a broadband IF matching is an active bufferstage (figure 4.3.1).

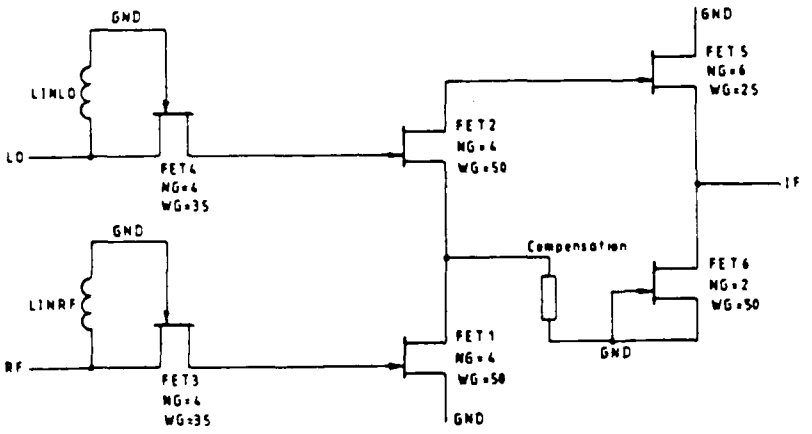


Figure 4.3.1 Adding the IF bufferstage completes the circuit.

The dimensions of both FETs determine the high frequency output resistance. This resistance is the parallel value of the rds of FET6 and the 1/gm of FET5. Due to the relative low frequency of the IF-band, parasitic capacitance is neglectable.
The current through the bufferstage determines the dimensions of both resistors. The FET dimensions are obtained with Touchstone simulation (chapter 6).

5 THE DIRECT CURRENT BEHAVIOUR OF THE MIXER.

In this chapter the d.c. behaviour is discussed and the influence of process variations on this. Also the temperature behaviour due to dissipation is calculated. The program Saber [3] is used for the calculations.

5.1 The DC setup

The final chip will be mounted in a case with two capacitors of 100pF. This restricts the allowed bias interconnections to a maximum of two. A GaAs FET normally is biased with a Vds between 2 and 4 volts. The Ids depends on the application of the FET in the circuit.

Both FETs at the input of the circuit, FET3 and FET4, have a Vgs of zero volts due to the inductor between source and gate. Therefore the current is equal to the saturation current Idss and is, for the chosen dimensions, 20mA.

FET1, which amplifies the RF signal, is adjusted to a relatif low current (for low noise figure) of one third of Idss. For the chosen dimensions Ids is 10mA.

The mixing FET (FET2) is biased in its non-linear region, close to the pinch-off voltage, therefore Ids is around 6mA.

The current through the bufferstage is determined by FET6. For the chosen dimensions Ids=Idss=15mA.

If the gate of FET3 is defined as a ground potential and Vplus1=10V and Vplus2=5V, the rest of the circuit will have the voltage levels as shown in figure 5.1.1 . A few resistors are added for providing proper bias levels. The LO and RF stage biasing are separated to prevent high frequency coupling between both stages.

The two required bias supplies are both positive and are decoupled with the two 100pF capacitors. A problem that arises with this biasing method is that the IF-signal sees both capacitors in series, so the lowerside of the IF frequencyband will be limited by an effective capacitance of 50pF. This capacitance is too small for reaching the 100 MHz lowerside limit of the IF band.
However, it is possible to lower the complete d.c. level with 5 volts. Then the two required bias supplies are of positive and negative value. Now one side of the IF bufferstage is at ground potential and the otherside at +5 volts. The bandwidth is now limited by a capacitor of 100pF. This results in a better lower limit than in the previous case.

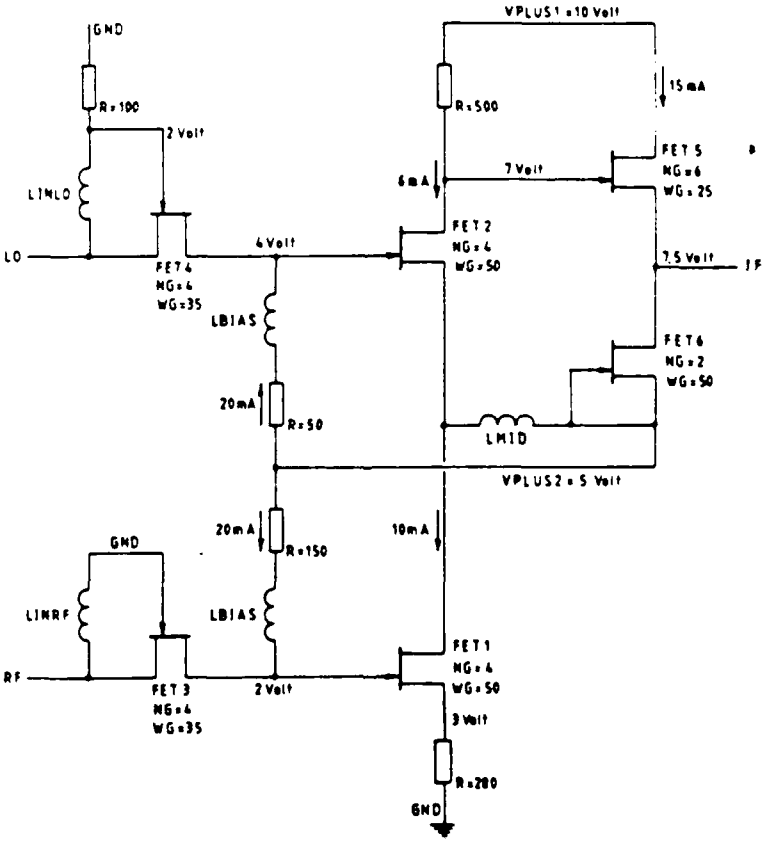


Figure5.1.1 DC levels with two positive power supplies.

Running ahead on a discussion of the possible consequences of process variations on the d.c. voltage and current levels in the circuit, a few resistors (or parts of them) have been replaced by FETs. If we mention here, that two FETs with the same dimensions are in series then, in spite of the current which flows through them, the voltage between drain and source will divide proportionally. Paragraph 5.2 discusses more details about process variations and the possible influences on the biasing.
The inductor LBIAS in the RF-stage is omitted due to the addition of FET7 which provides a high impedance for r.f.

The input inductors LINRF and LINLO have, due to material properties, a d.c. resistance of about 2.5 Ω. To compensate this, a similar resistor is added between the gates and sources of FET7 and FET8.

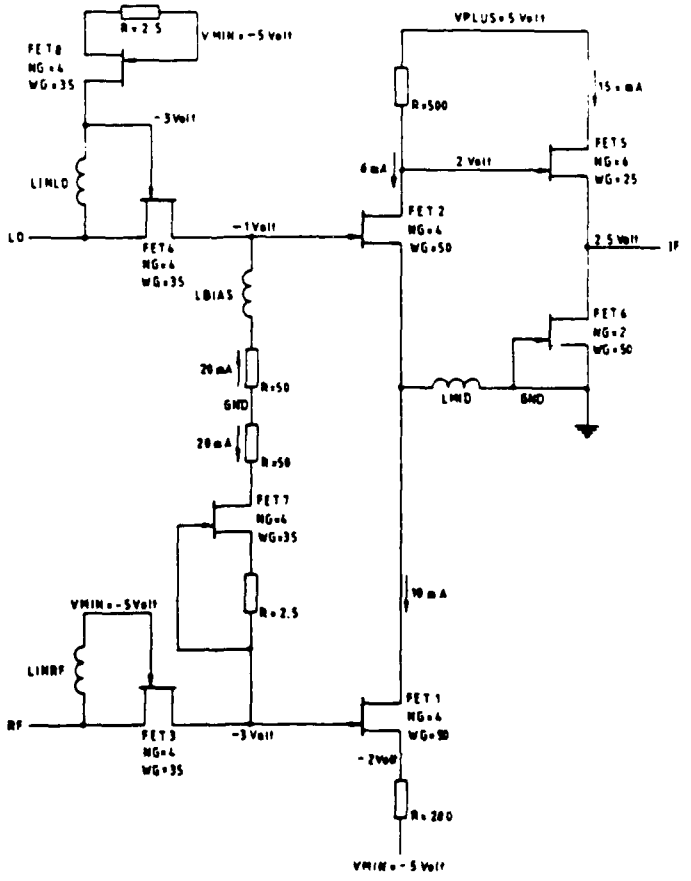


Figure 5.1.2 DC levels with a positive and a negative power supply

5.2 The influence of the process and the temperature on the d.c. behaviour.

It appears that the complete d.c. set up depends on the saturation current Idss of all FETs and on the resistors of 50, 280 and 500 Ω.

All used resistors are NiCr resistors. The maximum deviation (2-sigma values) from wafer to wafer is ±5% and the mutual matching on the chip is better than ±0.5%. Furthermore, the resistance of NiCr is virtually independent of temperature. From this it appears that only the deviation from wafer to wafer is important.

The influence of the proces on Idss is mainly determined by the deviation in the doping concentrations. The variables in the spice simulation model which determine Idss and depend on the doping concentration (Nd) are beta, lambda, |Vp|, Rs and Rd [2].
The following values are the 2-sigma values:

Idss	:: beta	:: Nd
Idss	:: lambda	:: Nd
Idss	:: |Vp|	:: Nd
Idss	:: 1/Rs and 1/ Rd	:: Nd

Maximum Idss:	beta	+10%	Minimum Idss:	beta	-10%
	lambda	+20%		lambda	-20%
	Vp	-0.2 volt		Vp	+0.2 volt
	Rs,Rd	-30%		Rs,Rd	+30%

Beta, Vp, Rs en Rd are also influenced by the temperature.

beta	-2500 ppm/deg
Vp	-1.9 mV/deg
Rs,Rd	+1200 ppm/deg

The influence of these parameters on the d.c. characteristic of a 50 μm FET is shown in figure 5.2.1.

The maximum current appears when Idss is maximal and the temperature is low (0 degrees centigrade). The minimum current appears when Idss is minimal and the temperature is high (70 degrees centigrade). It appears that the wafer to wafer variations are dominant.

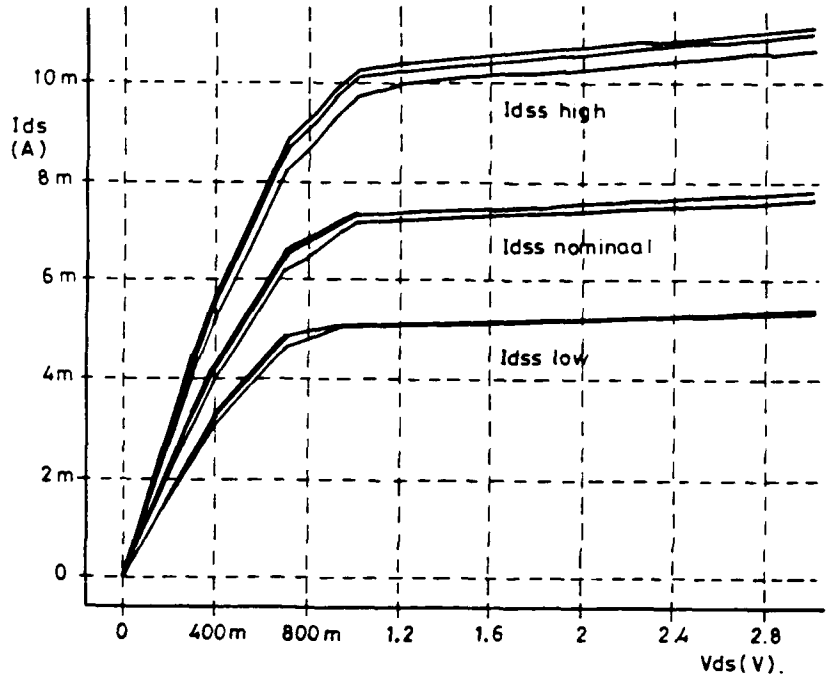


Figure 5.2.1 Influence of process and temperature on the dc behaviour of a 50 μm FET

If these parameters are used in the schematic diagram of figure 5.1.2 and it is presumed that each FET has the same variation of Idss and each resistor the same deviation, and the chip temperature is more or less constant, then the voltages and currents have the variations shown in the figures 5.2.2 to 5.2.4.

Those figures show that the d.c. points only shift unacceptable when in the process Idss is minimal. To adjust the d.c. points to normal values, we have to increase the 50 Ω resistor in the LO-stage to 60 Ω. See figure 5.2.5.
In the layout this resistor is made of three choosable resistors of 50, 55 and 60Ω.

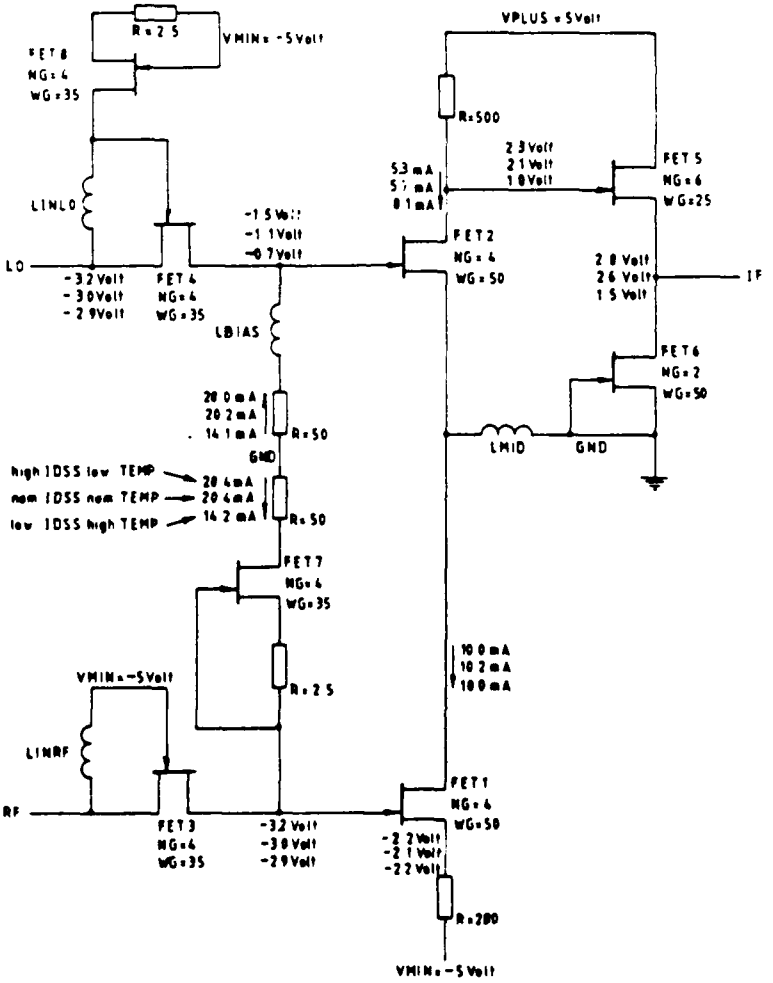


Figure 5.2.2 Influence of the process on the DC behaviour with normal resistor values

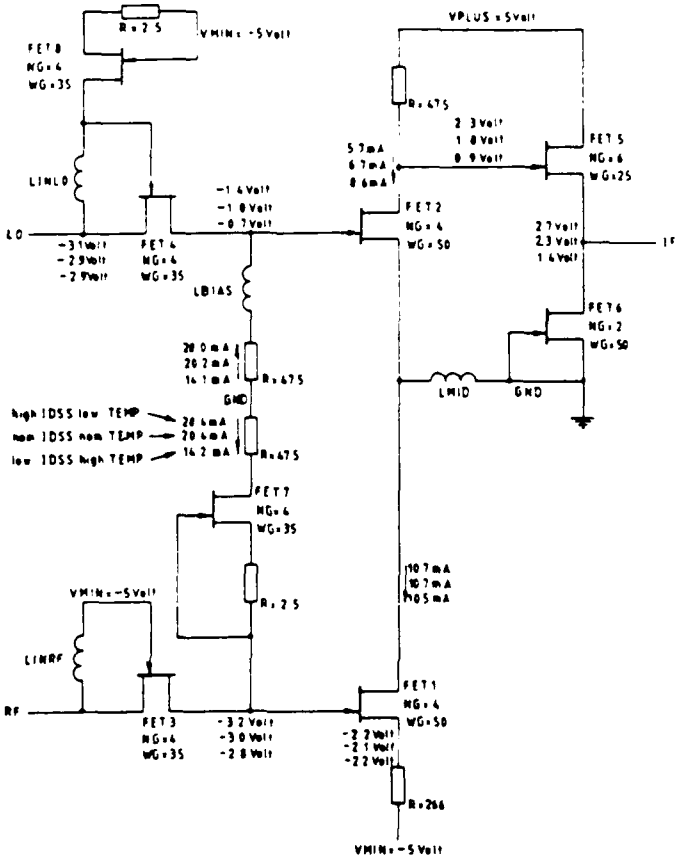


Figure 5.2.3 Influence of the process on the dc behaviour with low resistor values.

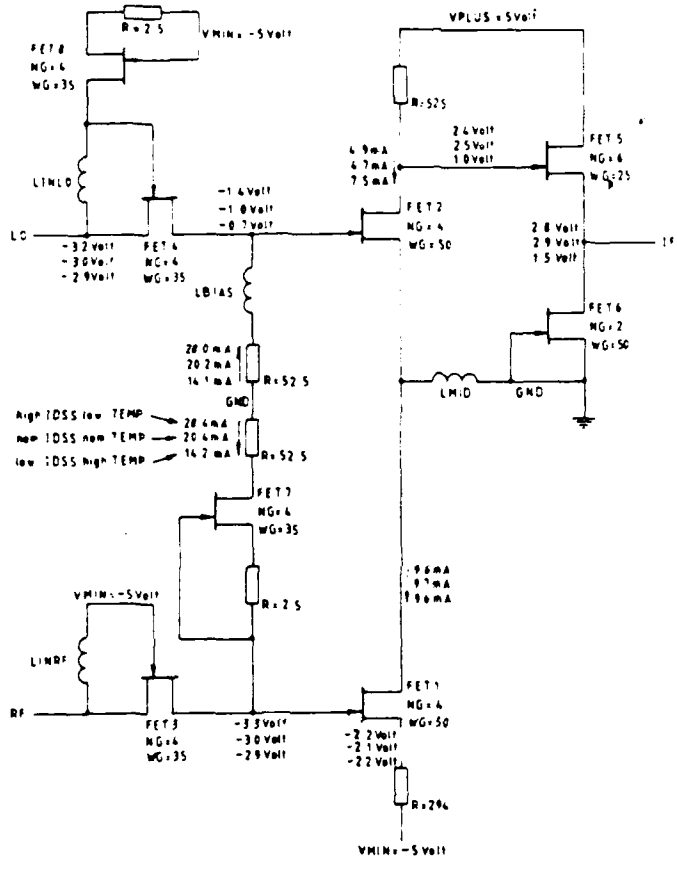


Figure 5.2.4 Influence of the process on the dc behaviour with high resistor values.

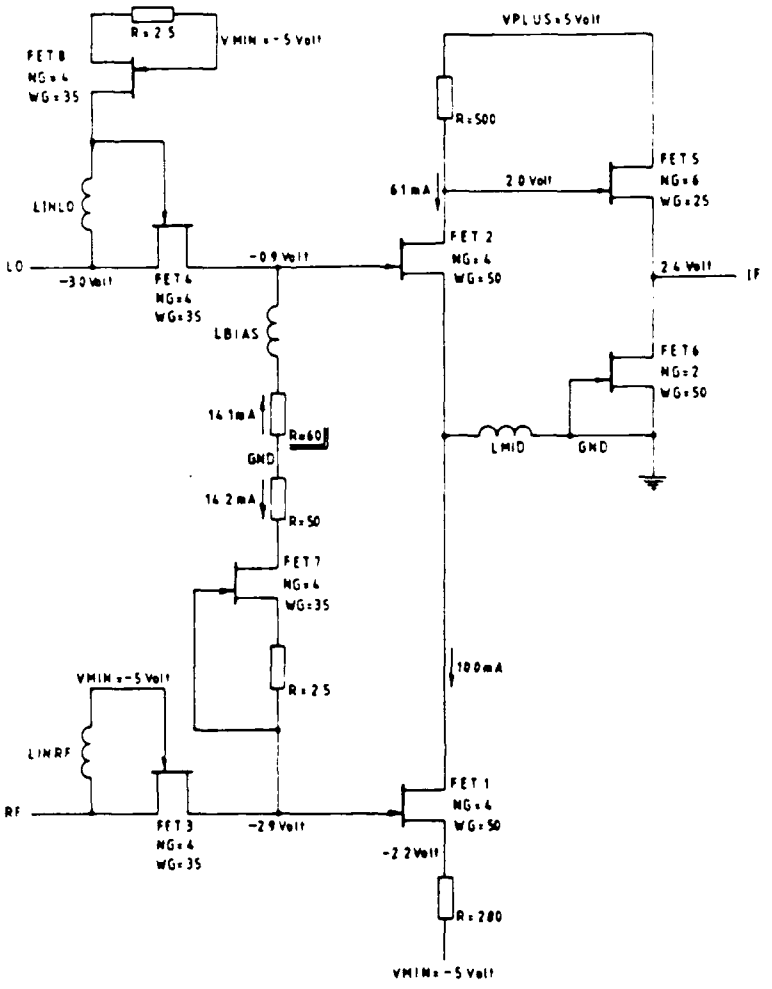


Figure 5.2.5 Correction on the dc behaviour with an adjustable resistor.

5.3 The temperature rise due to dissipation.

To determine the temperature rise of the dissipating componentents, two figures and some simple formulas are used.

First the temperature rise of the resistors is determined. The thermal impedance of rectangular resistors is expressed as:

$$\theta = .55 * \frac{Fa(l/w)}{k*\sqrt{l*w}}$$

Fa(l/w) is a correction factor for the ratio l/w and is given in figure 5.3.1.

k is the thermal conductivity of GaAs and is 46 W/m-°C.
l and w are the dimensions of the resistor.

In the HA-process of Triquint, a square resistor in NiCr is 50 Ω and the maximum current (due to migration) is 1mA/μm width.

to provide an analytical basis for such estimates.

In the paper by Joy and Schlig, it is shown that the maximum temperature can be expressed by a thermal impedance, Θ as follows:

$$\Theta = 1.1 \times \frac{F_a(l/w)}{2k\sqrt{lw}}$$

Where $F_a(l/w)$ is a shape factor depending only on the ratio l/w and which has a value near one. Joy and Schlig s computed values for F_a are presented in figure [illegible].

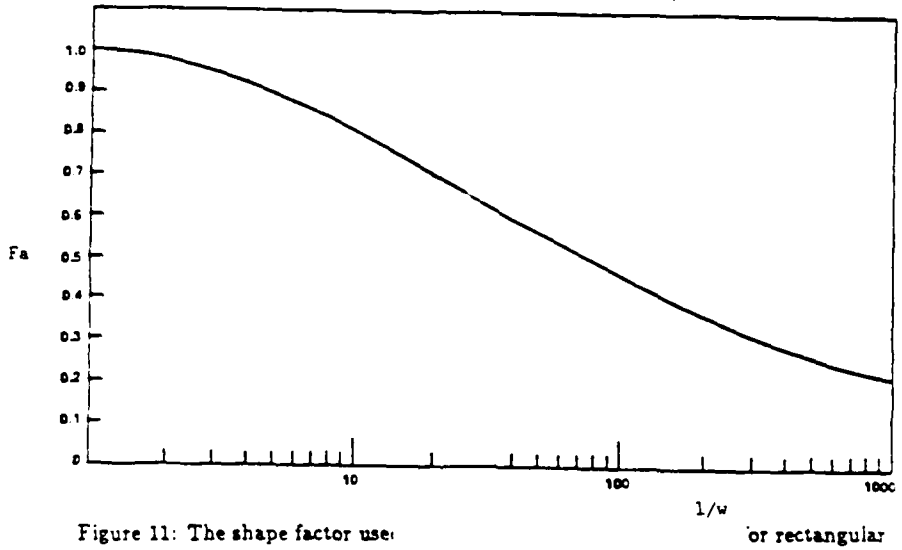


Figure 11: The shape factor use[illegible] or rectangular resistors. Taken from Joy and Schlig.

We have compared the results of this analysis with liquid crystal measurements for square rectancular resistors ranging in size from 5 x 5 *microns* to 225 x 225 *microns* and find general agreement with the Joy and Schlig model if we also include a slight

Figure 5.3.1 Correction factor for the thermal impedance of non-square resistors.

For the resistors in the circuit we get:

Both 50Ω resistors:
I=20 mA → P=20 mW
↓
w=l=40 μm → θ=300 °C/W
} $T_{rise} \approx$ 6 degrees.

Both 2.5Ω resistors:
I=20 mA → P=1 mW
↓
w=60 μm , l=3 μm → θ=624 °C/W
} $T_{rise} \approx$ 0.6 degrees.

The 280Ω resistor:
I=10 mA → P=28 mW
↓
w=20 μm , l=112 μm → θ=220 °C/W
} $T_{rise} \approx$ 6.2 degrees.

The 500Ω resistor:
I=6 mA → P=18 mW
↓
w=20 μm , l=193 μm → θ=158 °C/W
} $T_{rise} \approx$ 3 degrees.

The largest temperature rise is to be expected at the 280Ω resistor. That temperature increase is added to the total temperature increase of the GaAs chip with regard to the ambient temperature.
For the determination of the temperature rise of the FETs the average power per μm gate-width has to be calculated. With help of figure 5.3.2 the temperature increase of each FET is derived.

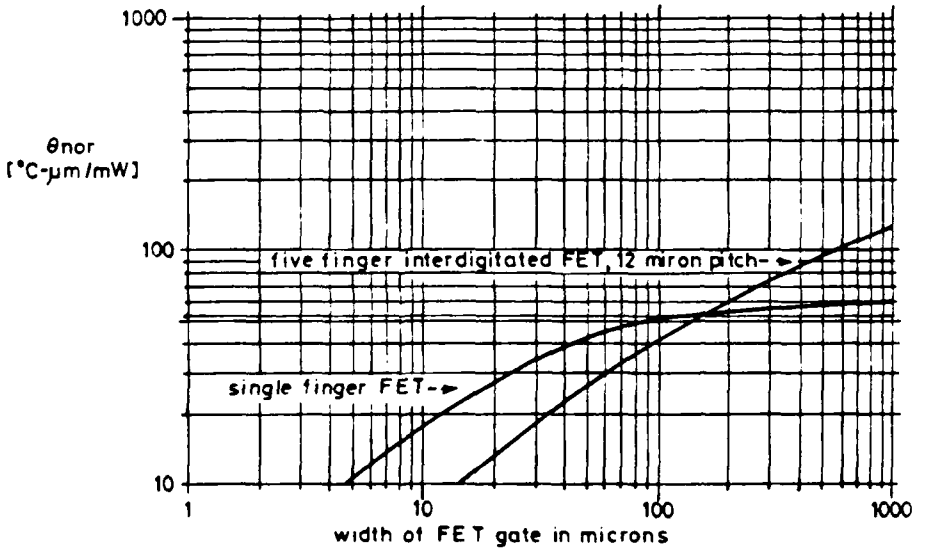


Figure 5.3.2 Normalized thermal impedance of two different FETs.

For the FETs in the circuit we get:

The 4x35=140μm FET (FET3,4,7,8):
Ids=20 mA, Vds=2 volt → Pgate=0.28 mW/μm
From figuur 5.3.2: θnor=50 °C-μm/mW
→ T_{rise} ≈14 degrees.

The 4x50=200μm FET in the RF-stage (FET1):
Ids=10 mA, Vds=2.2 volt → Pgate=0.11 mW/μm
From figuur 5.3.2: θnor=60 °C-μm/mW
→ T_{rise}≈6.6 degrees.

The 4x50=200μm mixer FET (FET2):
Ids=6 mA, Vds=2 volt → Pgate=0.06 mW/μm
From figuur 5.3.2: θnor=60 °C-μm/mW
→ T_{rise}≈3.6 degrees.

The 6x25=150μm FET in the bufferstage (FET5):
Ids=15 mA, Vds=2.5 volt → Pgate=0.25 mW/μm
From figuur 5.3.2: θnor=54 °C-μm/mW
→ T_{rise}≈13.5degrees.

The 2x50=100μm FET in the bufferstage (FET6):
Ids=15 mA, Vds=2.5 volt → Pgate=.375 mW/μm
From figuur 5.3.2: θnor=45 °C-μm/mW
→ T_{rise}≈ 17 degrees.

The largest temperature rise is to be expected in the 2x50 μm FET of the bufferstage.

The total dissipation of the chip is:

+5 volt * (6 mA + 15 mA)	=	105 mW
-5 volt * (20 mA + 20 mA + 10 mA)	=	250 mW +
Total		355 mW

The thermal resistance, according to Triquint, is 35-40°C/W. So the temperature rise of the chip will be ≈14°C.

The maximum peak temperature appears at the 2x50μm FET of the bufferstage. With an ambient temperature of 25°C, the peak temperature will be 25+14+17=56°C.

6 ANALYSIS AND OPTIMIZATION OF THE MIXER.

In this chapter the r.f. behaviour of the mixer with the aid of the linear simulation program Touchstone [2] and the non-linear program Saber [3] will be discussed .
Layout paracitics are not yet included (chapter 7 and 8).

6.1 Adding r.f. components to the d.c. circuit

The inductors between the gates and sources of FET3 and FET4, as shown in the d.c. circuit, have also a r.f. function. Signal loss through the inductors has to be avoided and therefore the inductors have to be as large as possible. However, due to the dimensions of the GaAs substrate (1.4 * 1.4 mm), only small inductors can be used. The inductor together with the gate-source capacitance of the FET forms a parallel resonant circuit. So a good value for the inductor is when this resonance happens around 10 GHz.

The inductor to ground between FET1 and FET2 provides a better matching for the gate of FET2 and also a d.c. ground level.
Also a few capacitors are added to the circuit, shown in figure 6.1.1. The capacitors connected to the gates of FET3 and FET4 make a short for the r.f. signal to ground, so a good matching (1/gm) is achieved. The value of the capacitors is 2.5pF. This value results in a manageable size on the GaAs substrate.
The capacitors at the inputs of the LO and RF provide a d.c. decoupling.

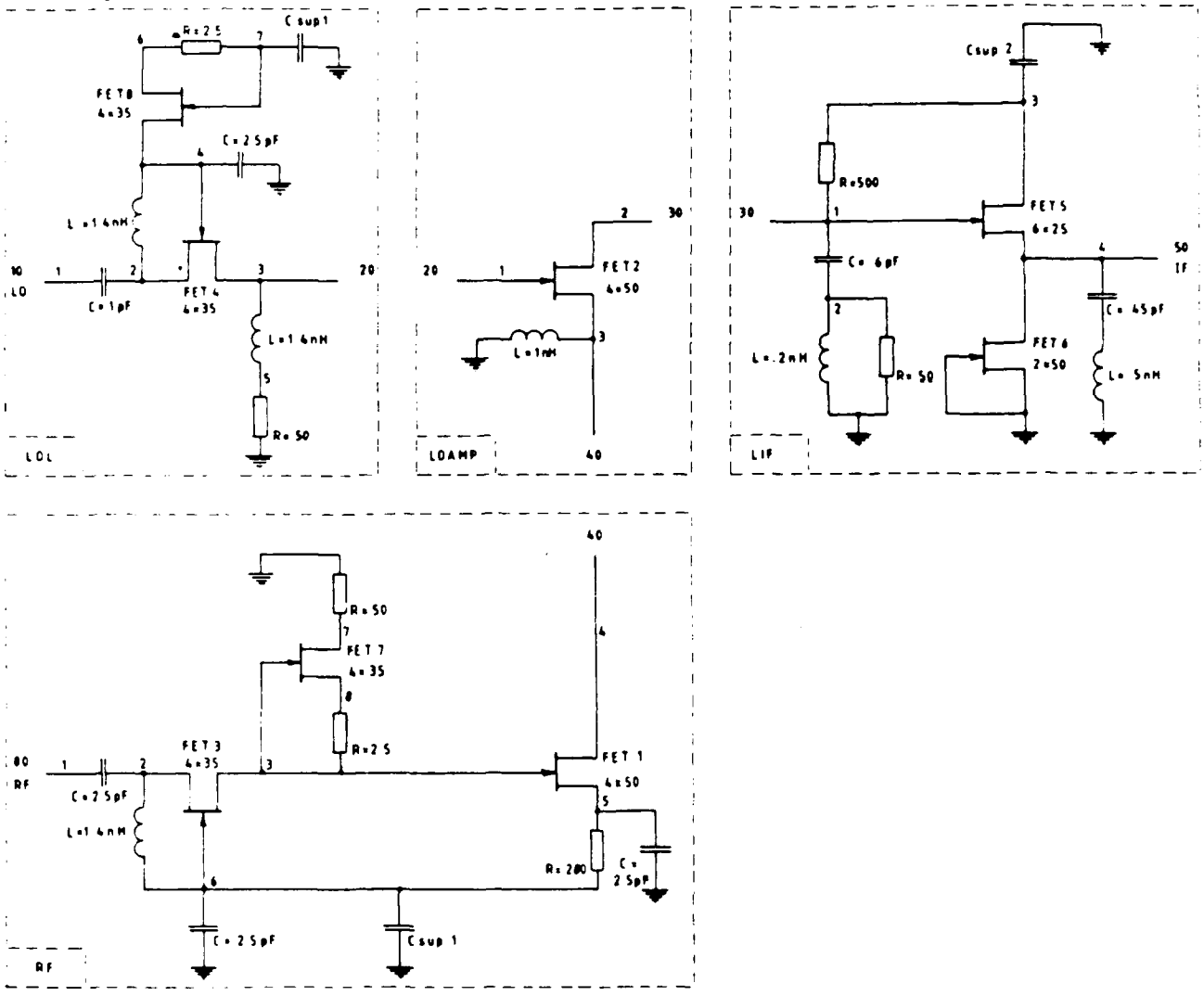


Figure 6.1.1 The complete circuit of the mixer.

6.2 Suppression of the LO-signal

For suppressing the LO-signal, that leaks through FET2, a filter is provided between FET2 and the IF bufferstage (see figure 6.1.1). First a parallel series resonator was applied which suppressed the LO band but it didn't give much attenuation at the second harmonic of the LO. A second possibility, a lowpass filter in series with the signal, gave

problems with matching the IF bufferstage and the input of the LO. A better solution is the use of a parallel highpass filter and dissipating the LO signal in a resistor. By adding a parallel series resonator at the output of the bufferstage, a good suppression for the LO band as well as the harmonics is achieved.

6.3 Linear analysis

The values used in figure 6.1.1 are derived after optimization with Touchstone . The circuit is, for use in Touchstone, divided in a few subcircuits. It is then possible, to simulate a part of the circuit while it is surrounded (as a source and/or load) with the remaining circuit. The simulation results are shown in the figures 6.3.1., 6.3.2 and 6.3.3. Figure 6.3.1 shows the input reflection and forward transmission of the RF and LO input-stages of the mixer. Figure 6.3.2 shows the output reflection and forward transmission of the IF-stage of the mixer at the IF frequency-band. Figure 6.3.3 shows the forward transmission of the IF-stage at higher frequencies. Due to the filter section the suppression of the LO and RF input signals and of the harmonic frequencies are good.

In addition the stability of the circuit is tested with the help of the stability factor K. It appears that some subcircuits are potentially unstable for certain frequencies. This means that the circuit can oscillate when there is a certain mismatch at the input and/or output of a (sub)circuit.
With the help of the stability circles (Touchstone) it is possible to determine when the input and/or output impedances are in- or outside the stable regions of the (sub)circuit. All the input and output impedances for the optimized subcircuits are well within the stable regions, therefore the circuit is stable.
The Touchstone circuit file is shown in appendix A (LAYMIX.CKT), including a table with the calculated S-parameters and the K-factors.

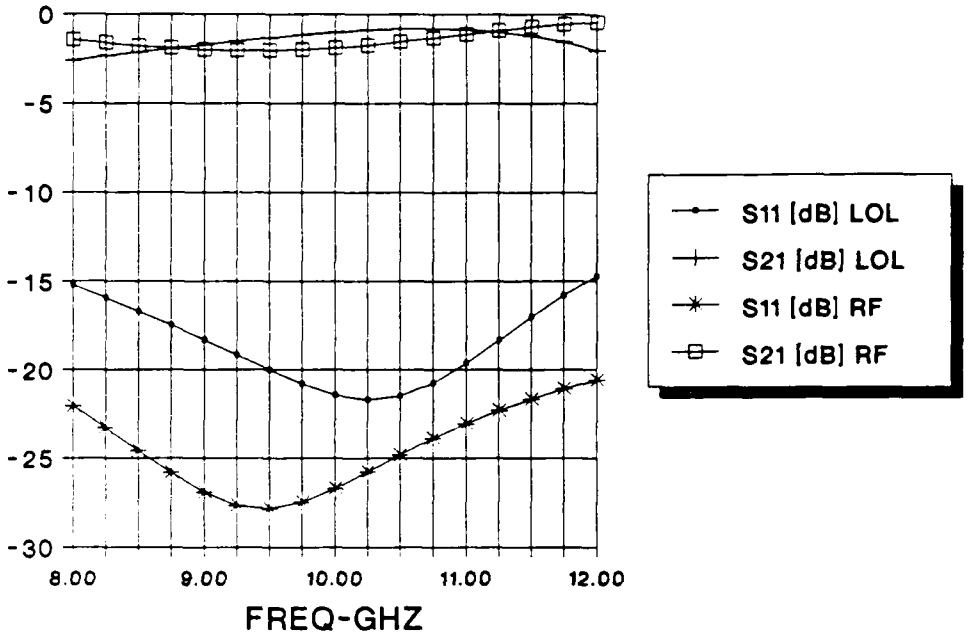


Figure 6.3.1 The input reflection and forward transmission of the subcircuits LOL and RF.

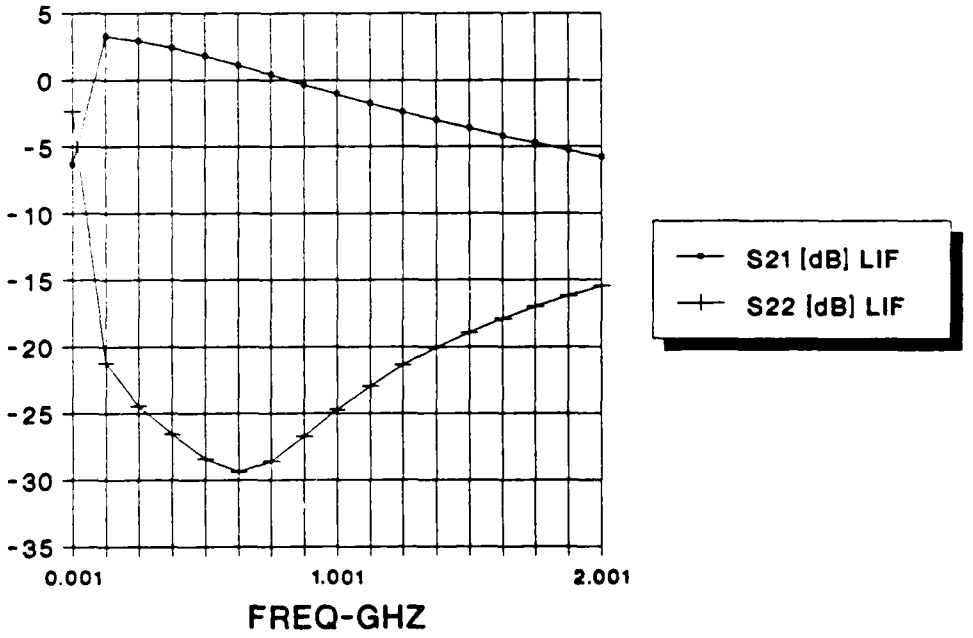


Figure 6.3.2 The output reflection and forward transmission of the subcircuit LIF as function of the IF-frequencyband.

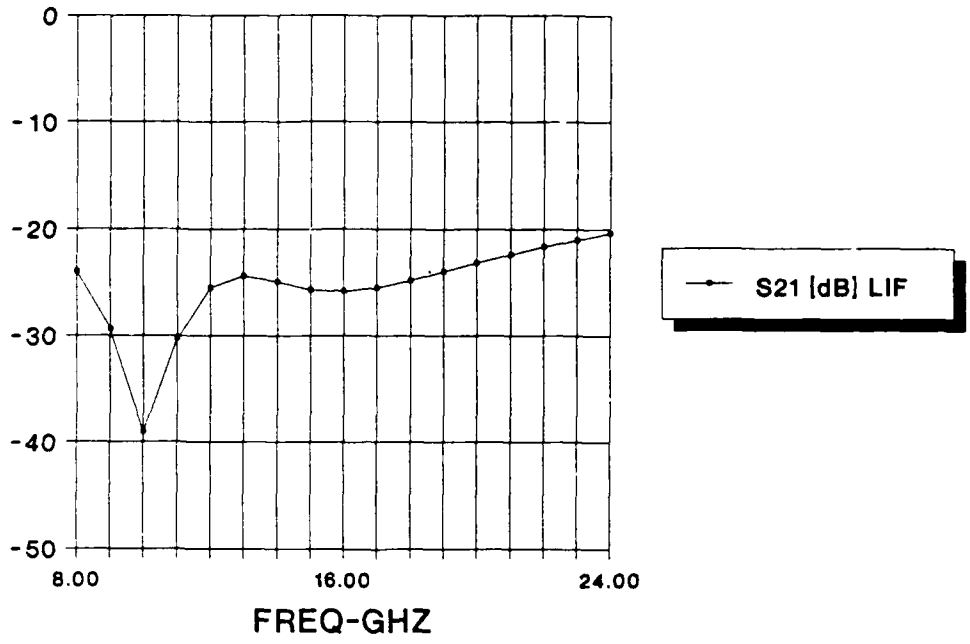


Figure 6.3.3 The forward transmission of the subcircuit LIF

6.4 Non-linear analysis

The computer program Saber is used for a non-linear analysis of the circuit. Saber is very limited in microwave analysis, so only conversion gain/loss is simulated.
A signal of 10.25 GHz (0dBm) is applied to the LO input and to the RF input a signal of 9.75 GHz (-20dBm). This provides an IF signal of 500 MHz.
Figure 6.4.1 shows the RF signal (top) and the IF signal (bottom). The 500MHz ripple on the RF signal is a feed-back effect of the IF stage to the RF stage of the circuit. The IF signal consists of 500 MHz, the second harmonic of the LO signal and the upper sideband which is 10.25 + 9.75 = 20GHz. The power output of the IF-signal amounts to -19dBm so there is a conversion gain of 1 dB.

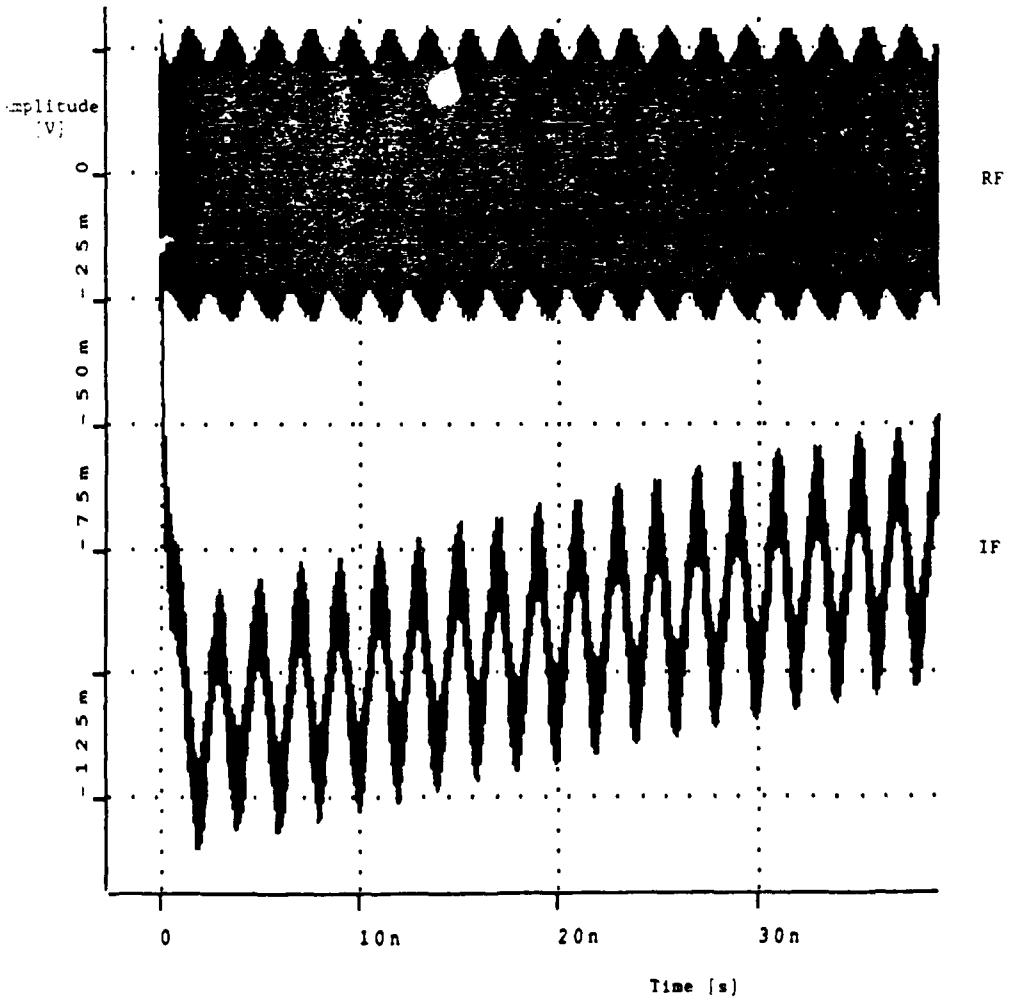


Figure 6.4.1 RF and IF signal of the mixer.

7 THE LAYOUT.

In this chapter the layout generation and the consequences for the high frequency behaviour is discussed.
The layout is made with the programm ICED [5]. This is a simple but, for this purpose, nice layout editor.

7.1 The initial layout.

A first difficulty that arises is that the HA-process doesn't allow any "via-holes" (connections through the substrate to ground). Therefore each groundpoint in the circuit must be transported by use of transmission lines to the edge of the substrate. A choice that was made is to divide the circuit into subcircuits with a groundplane surrounding it. This has two advantages, the effective length to ground becomes shorter and at the same time it provides some shielding between the subcircuits. Figure 7.1.1 shows the geography of the chip with all the elements placed on it. That gives an idea how many space the elements take.

Triquint provides various design rules for making a good layout, like maximum currents through the metal-layers and the NiCr resistor layer, spacing between layers and which layers have to overlap each other. It is not within the context of this report to discuss all the design rules.

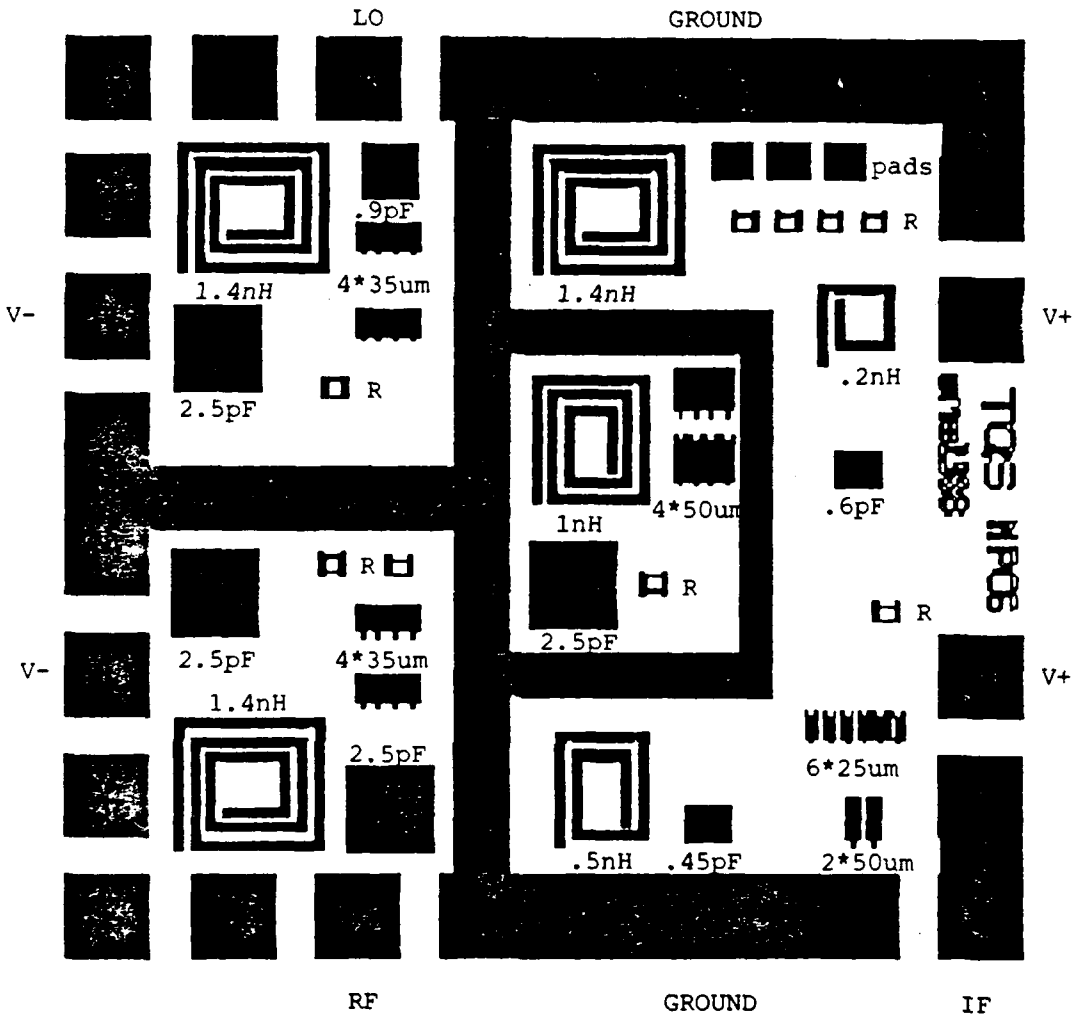


Figure 7.1.1. A rough placement of the elements on the chip.

7.2 The parasitics due to the layout

When the layout is finished, simulations with Touchstone have to be done. Due to the layout there are several microstrip lines added to the circuit. Also there are parasitic capacitances to ground. Because it is not possible to make via holes in the HA process, the groundlevel of the chip will be floating above the surrounding groundlevel due to bondingwires and microstrip lines. All these parasitics are defined during simulation as follows:

1. All connections made with the first metal layer will be modelled as microstrip lines. For the MSUB statement in Touchstone the following values are valid : Er=12.9, H=100μm, T=2μm, RHO=1 and RHG=0.

2. All connections made with the second metal layer will be modelled as inductors. With a width of 10μm the induction is $\approx$75pH/100μm. The induction of two connections in parallel gives about half the value of one connection.

3. The parasitic capacitance to ground of a bondingpad is $\approx$45fF/(100x100)μm^2. At one end of a capacitor (the "bottom" plate) there is also a parasitic capacitance to ground of about $\approx$45fF/(100x100)μm^2. The "top-plate" does not have this.

4. Connections from the chip to the surrounding world are done with bondingwires. These bondingwires are modelled as inductors, with a value of about 100pH/100μm.

7.3 Consequences of the layout on the r.f. behaviour of the circuit

It's of no use to discuss every step that was necessary to compensate for the layout parasitics. The most important consequences are mentioned

1. There is now a complex earth circuitry with bondingwires and microstrip lines wich connect the various components to ground.
2. Inductors to ground in the circuit appear to be larger. This means that the inductor value for the second harmonic filter in front of the IF bufferstage has to be decreased. Trying to reach the same performance, showed that the inductor became to small for realisation. The solution is a simple series resonant circuit. Due to the high frequency, the parasitic capacitance of a bondpad to ground is used, instead of a long ground path.
3. To decrease the RF-stage gain, a series inductor is included between the active input match and the FET.
4. Coupling between lines is not included, because it is very small according to Triquint and literature.
5. The subcircuits are connected to each other via a complex ground circuitry. For that reason it not possible anymore to simulate, with Touchstone, the individual behaviour of each subcircuit. In the next chapter this problem is discussed in more detail.

Figure 7.3.1 gives the total circuit with all the important layout parasitics, and in figure 7.3.2 a color plot is given of the definitive layout. Some testpoints and an extra FET, which can be measured with a wafer probe station are added. The results of the simulation will be discussed in the next chapter.

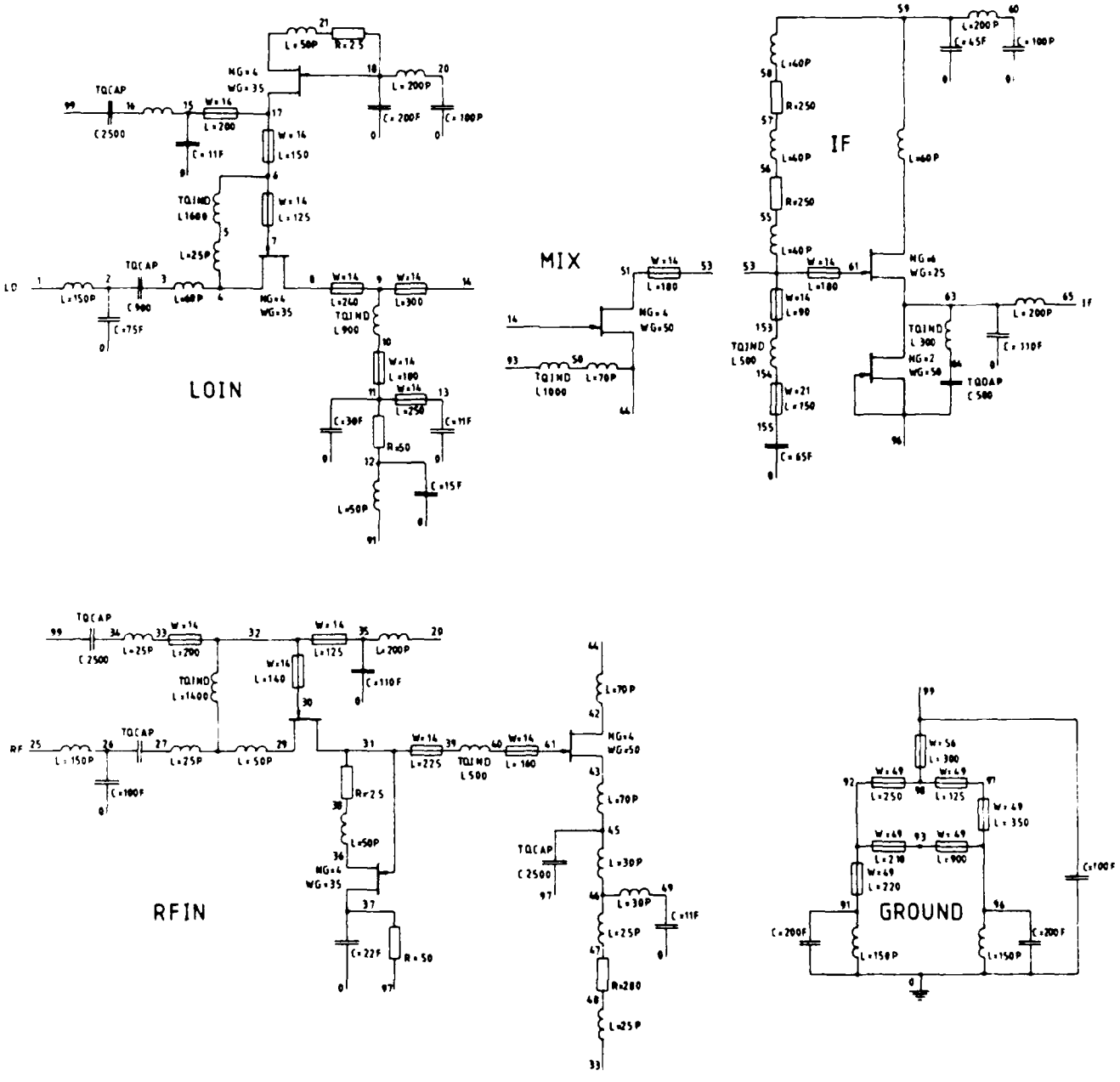


Figure 7.3.1 The complete circuit with all layout paracitics

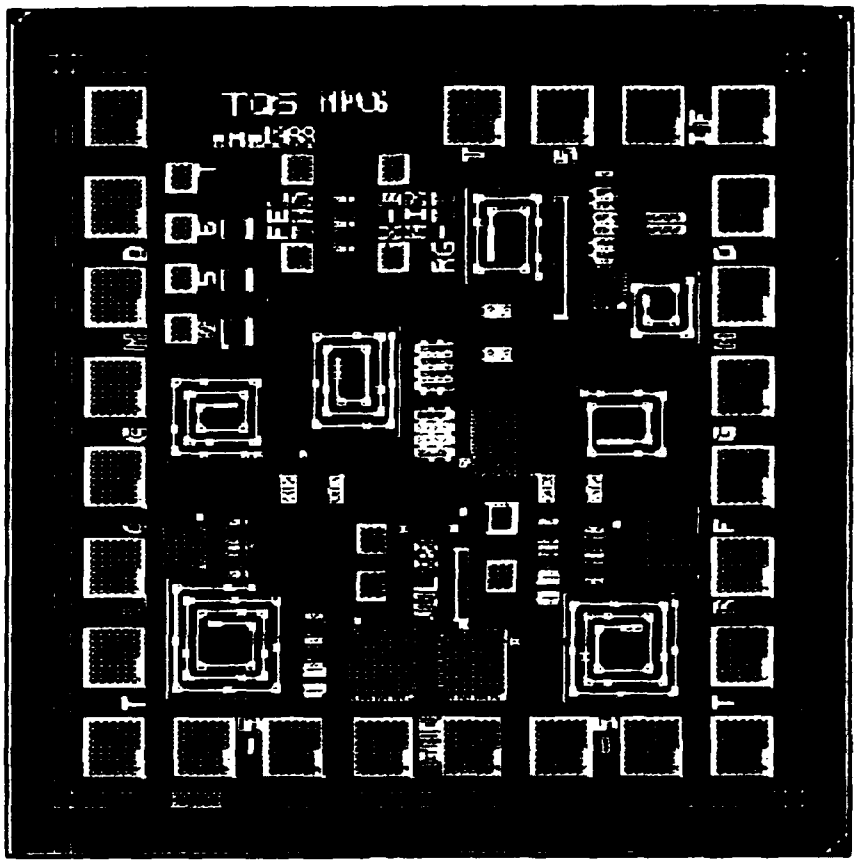


Figure 7.3.2 Color plot of the final layout.

8 THE SIMULATION RESULTS.

As mentioned in point 5 of paragraph 7.3, it is no longer valid to split the whole circuit into subcircuits, each with its own earth circuitry. In this chapter an other method to simulate the internal gains and stability of the circuit is discussed . A more detailed description of this method is given in [6].

8.1 The gain and the input and output return loss of the circuit

Figure 8.1.1 shows that there is a difference in return loss between the results of a divided circuit with more than one ground circuit and the same circuit with one common ground.
It is obvious that also the internal gains which are simulated with subcircuits are not correct.

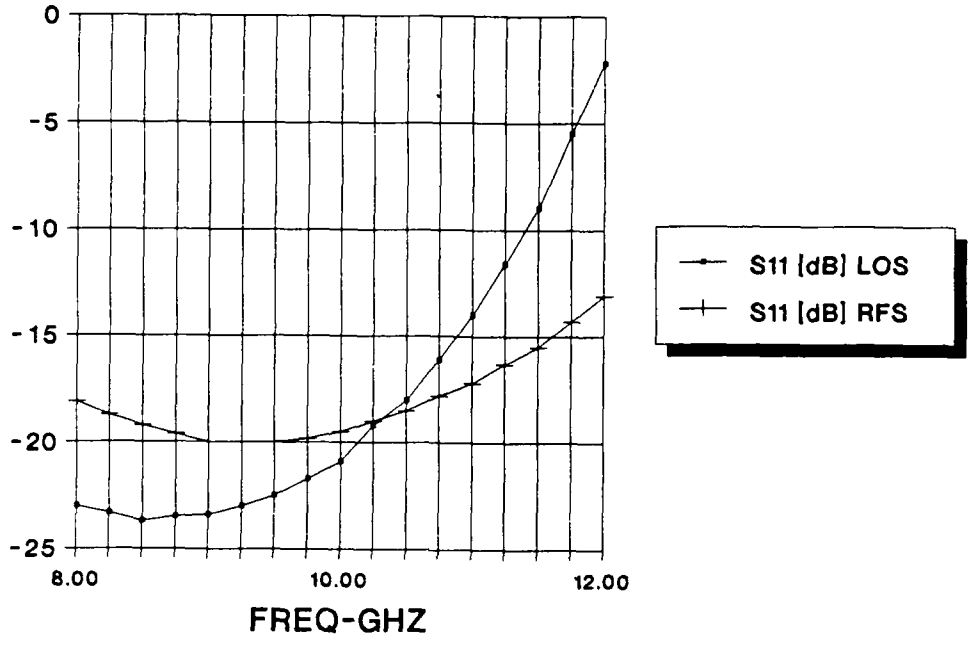
With Touchstone it is possible to calculate the relative voltage gain from the input to any other point in your circuit, with an ideal voltage controlled voltage source [7]. In a similar way it is possible to calculate the relative current gain at that point with an ideal current controlled current source.
The real power on that point is now defined as [6]:

$$Preal = | S21vol*S21cur | * \cos(\theta vol - \theta cur).$$

S21vol, S21cur are voltage and current gain
θvol, θcur are voltage and current phase.

With power measured at different nodes, gain can be simulated.
With this method it is possible to calculate voltages, currents and power without splitting up the circuit.
However, there is one problem. Touchstone can't make mathematical calculations like the cosine function. With the graphical interface of Saber it can, so datapoints, have to be transported from Touchstone to Saber to use this method.

The final results of the simulations of the circuit of figure 7.3.1 are given in the following figures. For data output etc. see appendix B.



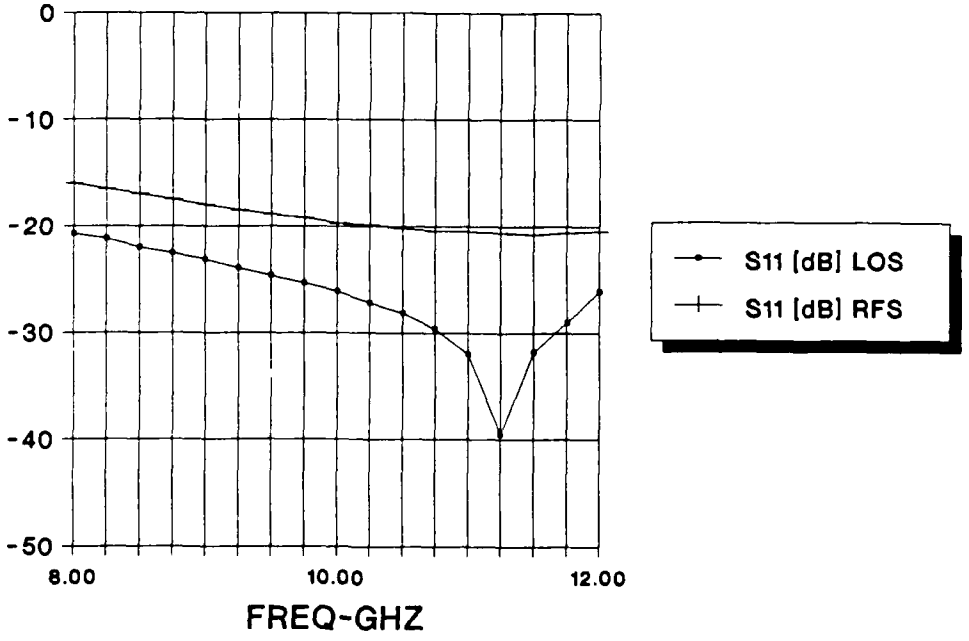


Fig.8.1.1 Simulation results of the return loss of the mixer with,
a) divided circuit with more than one ground circuit
b) total circuit with one common ground

Figure 8.1.2 gives the input return loss of the LO and RF input and the isolation from LO input to the RF input and IF output.
Figure 8.1.3 gives the gain of the RF and LO input to the mixing FET. These data is calculated with the above mentioned method.
Figure 8.1.4 gives the return loss of the IF output.
Figure 8.1.5 finally gives the gain of the IF bufferstage calculated with the above mentioned method.

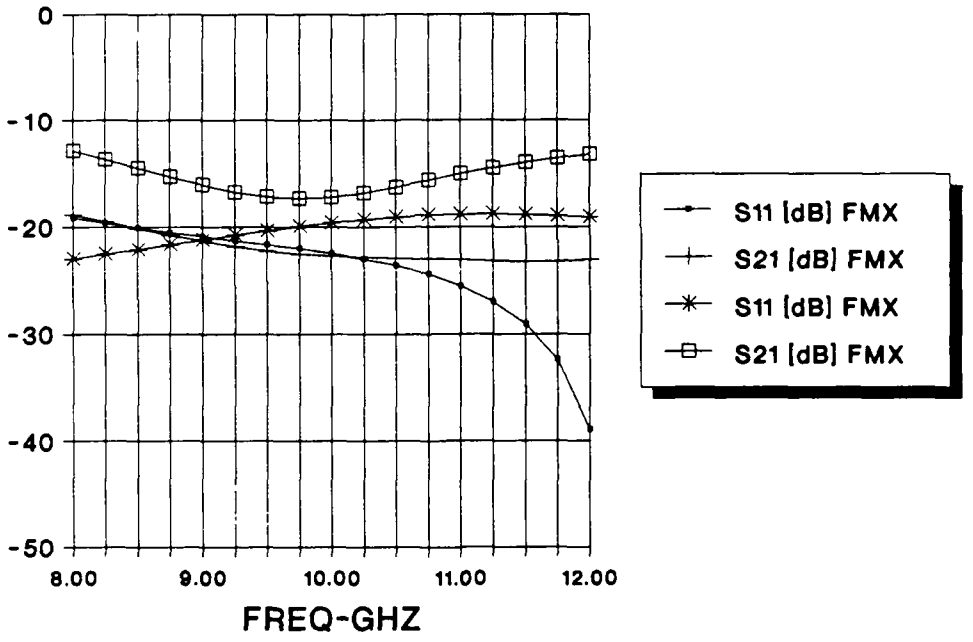


Figure 8.1.2 Input return loss and isolation of the final circuit.

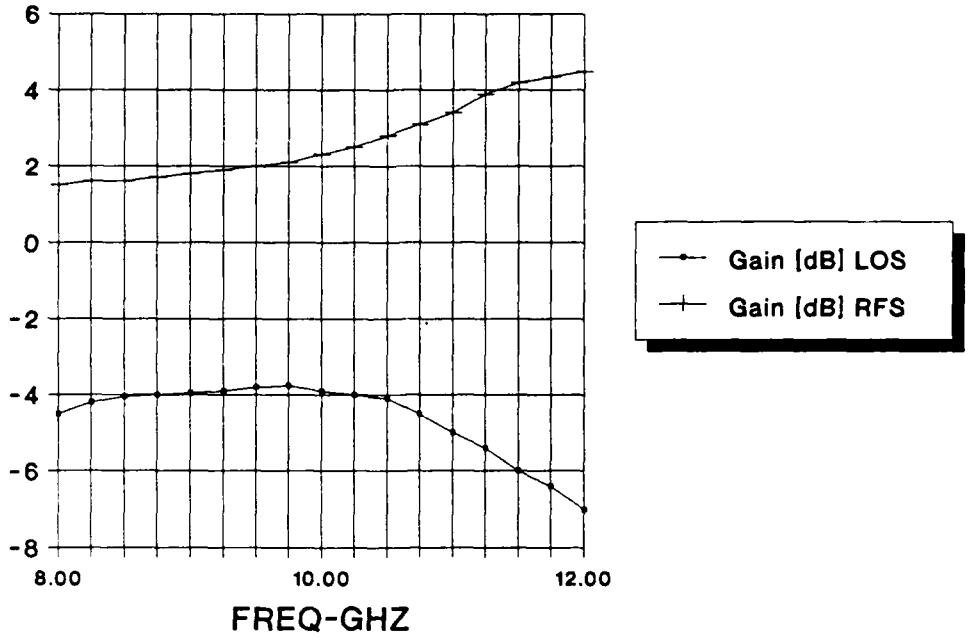


Figure 8.1.3 Gain from the RF and LO stage.

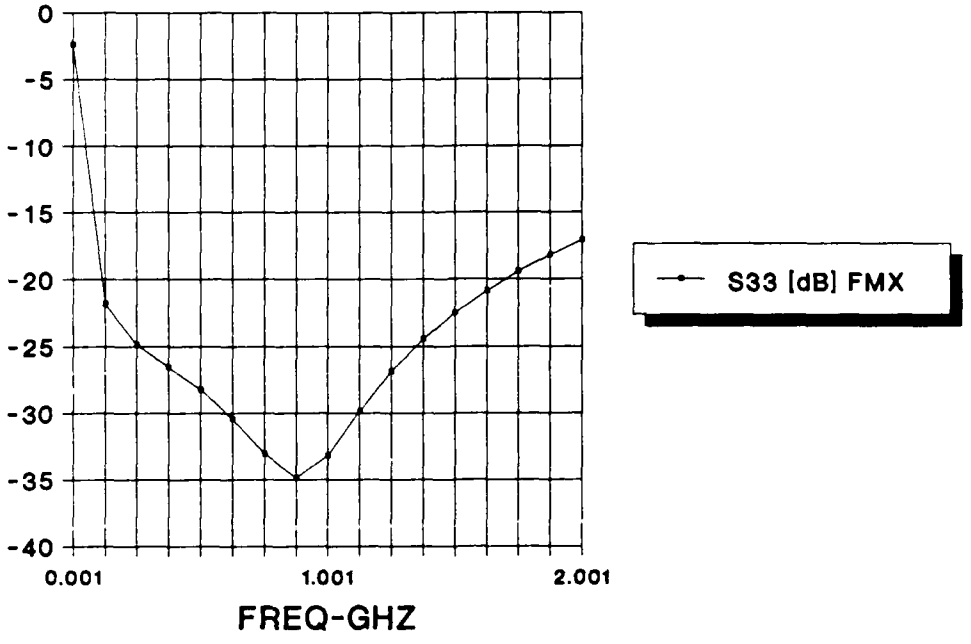


Figure 8.1.4 Output return loss of the final circuit.

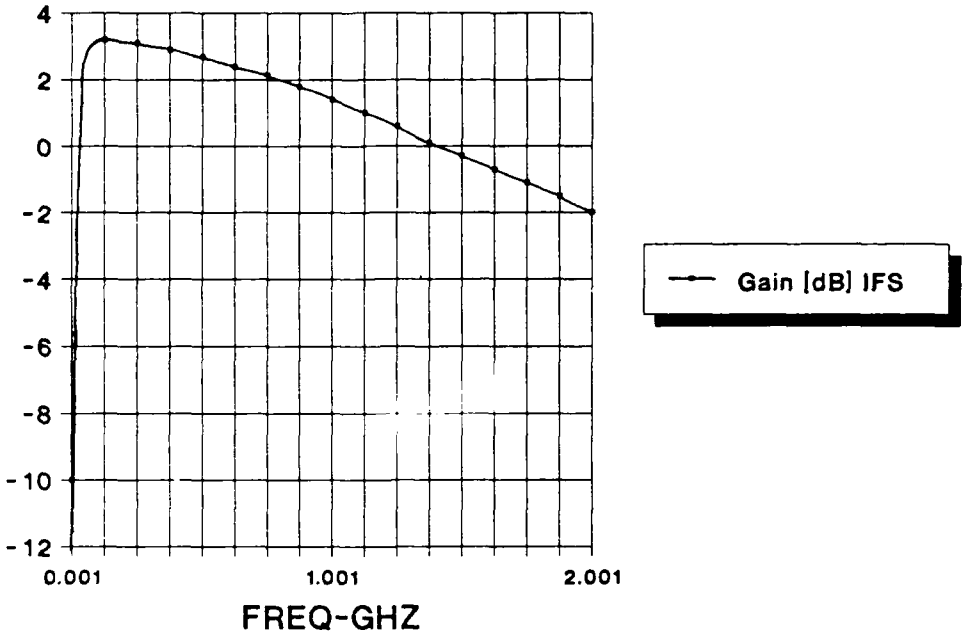


Figure 8.1.5 Gain from the IF bufferstage.

8.2 Stability of the circuit.

The stability factor and the stability circles of the whole circuit have been calculated. See Touchstone file MIXERKFA.CKT, appendix C.

It appears that around 16 GHz and 21 GHz we have a potentially unstable circuit. However with impedances of around 50 ohm the circuit is stable. Because it is a complex circuit, this will not guarantee that internal stages don't oscillate.
With the method of paragraph 8.1 also instability can be found. If the phase difference between voltage and current is more than plus or minus 90 degrees, there is a negative resistance at that point and the circuit will oscillate. The results of the simulations, appendix B, show that again around 16 GHz and 21 GHz phase differences greater than -90°appear. These phase differences appear after the active input match of the LO stage and at the input of the IF bufferstage. This is probably due to parallel and series resonance of the attached bonding ires for the earth and dc, with the (parasitic) capacitors on the chip.
Due to lack of time it was not possible to determine which bondingwires had to be smaller or larger.
It is possible, however, that the circuit will not oscillate after all, because not all parasitics are represented, the models used may not be accurate enough and the effect of packaging is not included. Because the gain of the active devices is dropping fast at the concerned frequencies, this may also suppress oscillation.

9 REMARKS AND CONLUSIONS.

The complete design and layout are established in a short time period, from the end of April till July 15, the deadline for the layout. For this reason it was not possible to compare and analyse different kinds of mixer principles.
The d.c. biasing and the r.f. behaviour are thoroughly simulated with respectively Saber [4] and Touchstone [3]. The non-linear behaviour, however, has not been simulated properly, because of the bad non-linear performance of Saber and the inadequate models for the active devices. Also the noise behaviour has not been dealt with because of the lack of noise models. For future designs it is necessary to have non-linear design tools and proper models available.

During the design, a new method is developed for simulating gain and stability of a complex circuit, like a MMIC with multiple ground paths.

In the second report an overall conclusion will be given.

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(Groupleader)

Ing. T.C.B. Tieman
(Author)

Ing. G. Grooters
(Author)

10 REFERENCES.

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[2] GaAs IC Design Course, Notes. Triquint Semiconductor.

[3] EEsof, TOUCHSTONE, a microwave computer aided design program, version 1.60

[4] Analogy, SABER, a design tool for analog systems

[5]. IC editors, Inc., ICED, an affordable Integrated Cicuit Editor, version 1.2

[6] New method to analyze stability and gain of MMIC designs. R. Grooters, T.C.B. Tieman. EEsof Users' Group meeting, 4 September 1989

[7] EEsof, Application note 2, Determination of node voltages within circuit, Chuck Holmes, Dave Morton

Appendix A

TOUCHSTONE LISTING AND SIMULATION RESULTS OF THE INITIAL CIRCUIT.

LAYMIX.CKT

```
DIM
        LNG     UM
        FREQ    GHZ
        CAP     PF
        IND     NH

CKT
        IND     2 3     L=.164
        IND     4 2     L=.024
        RES     1 2     R=3.43
        RES     1 4     R=.57
        CAP     1 3     C=.012
        DEF2P   1 3     L200

        IND     2 3     L=.499
        IND     4 2     L=.056
        RES     1 2     R=8.75
        RES     1 4     R=1.46
        CAP     1 3     C=.016
        DEF2P   1 3     L500

        IND     2 3     L=1.150
        IND     4 2     L=.200
        RES     1 2     R=17.78
        RES     1 4     R=2.96
        CAP     1 3     C=.028
        DEF2P   1 3     L1300

        IND     2 3     L=1.242
        IND     4 2     L=.197
        RES     1 2     R=17.15
        RES     1 4     R=2.86
        CAP     1 3     C=.026
        DEF2P   1 3     L1400

        IND     2 3     L=.973
        IND     4 2     L=.152
        RES     1 2     R=14.00
        RES     1 4     R=2.33
        CAP     1 3     C=.023
        DEF2P   1 3     L1000

        TQCAP   1 2     TYPE=1  C=1000
        TQFET   4 3 2   TYPE=2  W=35    N=4   XIDS=1     VDS=2    STAT=1
        L1400   2 4
        TQCAP   4 0     TYPE=1  C=2500
        TQFET   7 4 6 TYPE=2  W=35    N=4   XIDS=1     VDS=2    STAT=1
        RES     6 7     R=2.5
        CAP     7 0     C=100
        L1400   3 5
        TQRES   5 0     TYPE=1  R=50    W=40    H=7
```

LAYMIX.CKT

```
DEF2P   1 3     LOL

TQCAP   1 2     TYPE=1  C=2500
TQFET   6 3 2   TYPE=2  W=35    N=4   XIDS=1     VDS=2    STAT=1
L1400   2 6
TQCAP   6 0     TYPE=1  C=2500
CAP     6 0     C=100
TQFET   3 7 8   TYPE=2  W=35    N=4   XIDS=1     VDS=2    STAT=1
RES     8 3     R=2.5
TQRES   7 0     TYPE=1  R=50    W=40    H=7
TQFET   3 4 5   TYPE=2  W=50    N=4   XIDS=.33   VDS=2.1  STAT=1
TQRES   5 6     TYPE=1  R=280   W=20    H=7
TQCAP   5 0     TYPE=1  C=2500
DEF2P   1 4     RF

TQFET   1 2 3   TYPE=2  W=50    N=4   XIDS=.17   VDS=2.3  STAT=1
CAP     4 0     C=100
L1000   3 0
DEF3P   1 2 3   LOAMP

TQCAP   1 2     TYPE=1  C=600
L200    2 0
TQRES   2 0     TYPE=1  R=50    W=10   H=7
TQRES   1 3     TYPE=1  R=500   W=10   H=7
TQFET   1 3 4   TYPE=2  W=25    N=6   XIDS=.66   VDS=2.3  STAT=1
TQFET   0 4 0   TYPE=2  W=50    N=2   XIDS=1     VDS=2.7  STAT=1
TQCAP   4 5     TYPE=1  C=450
L500    5 0
CAP     3 0     C=100
DEF2P   1 4     LIF



LOAMP   20 30 40
LIF     30 50
MATCH   50
RF      60 40
MATCH   60
DEF1P   20      LOAD1

LOL     10 20
MATCH   10
LOAMP   20 30 40
LIF     30 50
MATCH   50
DEF1P   40      LOAD2

LOL     10 20
MATCH   10
LOAMP   20 30 40
RF      60 40
MATCH   60
DEF1P   30      LOAD3
```

LAYMIX.CKT

```
TERM
        LOL      0 0     LOAD1
        RF       0 0     LOAD2
        LIF      LOAD3   0 0

OUT
        LOL      DB[S11]     GR1
        LOL      DB[S21]     GR1
        RF       DB[S11]     GR1
        RF       DB[S21]     GR1
        LIF      DB[S21]     GR2
        LIF      DB[S21]     GR3
        LIF      DB[S22]     GR3

FREQ
        SWEEP    .001 2.001 .25
        SWEEP     8   12 .5
        SWEEP     12 24 1

GRID
        RANGE  8 12 .5
        GR1   -30 10 5
        RANGE  8    24    1
        GR2   -30 10 5
        RANGE .001 2.001 .25
        GR3   -30 10 5

OPT
        RANGE    8 12
        LOL  DB[S11]<-15  10
        RF   DB[S21]>0     5
        LOL  DB[S21]>0
        RANGE    8 24
        LIF  DB[S21]<-15   10
        RANGE    .001 1.5
        LIF  DB[S21]>0
```

LAYMIX.OUT

FREQ-GHZ	DB[S11] LOL	DB[S21] LOL	DB[S11] RF	DB[S21] RF	DB[S21] LIF	DB[S21] LIF	DB[S22] LIF
0.00100	-1.8e-05	-120.650	-8.5e-05	-74.159	-6.365	-6.365	-2.310
0.25100	-0.143	-52.688	-0.033	-41.542	2.949	2.949	-24.468
0.50100	-0.147	-48.798	-0.128	-28.776	1.821	1.821	-28.436
0.75100	-0.116	-46.134	-0.286	-19.658	0.413	0.413	-28.630
1.00100	-0.074	-39.599	-0.516	-13.106	-1.015	-1.015	-24.733
1.25100	-0.034	-33.766	-0.839	-8.365	-2.359	-2.359	-21.400
1.50100	-0.008	-29.190	-1.280	-4.991	-3.596	-3.596	-18.924
1.75100	-0.014	-25.475	-1.842	-2.650	-4.729	-4.729	-17.007
2.00100	-0.067	-22.362	-2.502	-1.062	-5.772	-5.772	-15.453
8.00000	-15.203	-2.596	-22.051	-1.423	-23.981	-23.981	-1.770
8.50000	-16.693	-2.131	-24.564	-1.772	-26.303	-26.303	-1.346
9.00000	-18.294	-1.700	-26.910	-1.991	-29.364	-29.364	-1.037
9.50000	-19.985	-1.314	-27.839	-2.035	-33.818	-33.818	-0.862
10.0000	-21.411	-1.001	-26.714	-1.881	-39.021	-39.021	-0.835
10.5000	-21.488	-0.815	-24.809	-1.549	-35.108	-35.108	-0.969
11.0000	-19.629	-0.842	-23.058	-1.113	-30.273	-30.273	-1.265
11.5000	-17.024	-1.204	-21.663	-0.700	-27.282	-27.282	-1.717
12.0000	-14.690	-2.039	-20.577	-0.450	-25.518	-25.518	-2.307
13.0000	-11.684	-5.677	-18.861	-0.729	-24.399	-24.399	-3.828
14.0000	-10.338	-16.616	-17.260	-1.817	-24.936	-24.936	-5.665
15.0000	-9.736	-10.998	-15.785	-3.163	-25.660	-25.660	-7.675
16.0000	-9.393	-9.822	-14.524	-4.476	-25.852	-25.852	-9.725
17.0000	-9.133	-10.041	-13.466	-5.674	-25.478	-25.478	-11.651
18.0000	-8.899	-10.760	-12.572	-6.750	-24.783	-24.783	-13.238
19.0000	-8.675	-11.776	-11.807	-7.718	-23.974	-23.974	-14.299
20.0000	-8.458	-13.071	-11.145	-8.592	-23.159	-23.159	-14.820
21.0000	-8.246	-14.750	-10.565	-9.389	-22.382	-22.382	-14.978
22.0000	-8.042	-17.164	-10.051	-10.119	-21.658	-21.658	-15.003
23.0000	-7.845	-21.910	-9.594	-10.792	-20.992	-20.992	-15.061
24.0000	-7.656	-23.089	-9.185	-11.420	-20.382	-20.382	-15.245

LAYMIX.OUT

FREQ-GHZ	K LOL	K RF	K LIF
0.00100	27.710	2.054	1.143
0.25100	50.411	5.564	152.582
0.50100	55.901	3.795	13.117
0.75100	42.284	4.566	7.230
1.00100	14.793	3.944	5.137
1.25100	3.410	4.233	4.032
1.50100	-0.150	4.948	3.345
1.75100	0.098	5.759	2.876
2.00100	3.290	6.592	2.537
8.00000	5.693	18.337	2.743
8.50000	5.043	18.714	3.808
9.00000	4.477	19.042	6.509
9.50000	3.985	19.327	16.963
10.0000	3.555	19.575	63.385
10.5000	3.178	19.791	35.720
11.0000	2.847	19.978	18.241
11.5000	2.556	20.140	14.206
12.0000	2.299	20.281	13.595
13.0000	1.869	20.507	15.842
14.0000	1.528	20.675	19.739
15.0000	1.255	20.797	22.526
16.0000	1.035	20.883	22.076
17.0000	0.855	20.942	19.095
18.0000	0.707	20.980	15.569
19.0000	0.584	21.000	12.559
20.0000	0.482	21.008	10.257
21.0000	0.396	21.007	8.545
22.0000	0.323	20.997	7.268
23.0000	0.262	20.983	6.301
24.0000	0.210	20.965	5.556

TOUCHSTONE LISTING AND SIMULATION RESULTS OF THE COMPLETE CIRCUIT WITH ALL PARASITIC COMPONENTS.

MIXERDEF.CKT

```
DIM
        LNG     UM
        FREQ    GHZ
        CAP     PF
        IND     NH

CKT
        MSUB    ER=12.9 H=100 T=2 RHO=1 RGH=0

        IND     2 3     L=.318
        IND     4 2     L=.034
        RES     1 2     R=5.82
        RES     1 4     R=0.97
        CAP     1 3     C=.012
        DEF2P   1 3     L300

        IND     2 3     L=.499
        IND     4 2     L=.056
        RES     1 2     R=8.75
        RES     1 4     R=1.46
        CAP     1 3     C=.016
        DEF2P   1 3     L500

        IND     2 3     L=.837
        IND     4 2     L=.113
        RES     1 2     R=13.58
        RES     1 4     R=2.26
        CAP     1 3     C=.025
        DEF2P   1 3     L900

        IND     2 3     L=0.973
        IND     4 2     L=.152
        RES     1 2     R=14.00
        RES     1 4     R=2.33
        CAP     1 3     C=.023
        DEF2P   1 3     L1000

        IND     2 3     L=1.242
```

MIXERDEF.CKT

```
IND      4 2     L=.197
RES      1 2     R=17.15
RES      1 4     R=2.86
CAP      1 3     C=.026
DEF2P    1 3     L1400

IND      2 3     L=1.364
IND      4 2     L=.233
RES      1 2     R=19.95
RES      1 4     R=3.33
CAP      1 3     C=.035
DEF2P    1 3     L1600


! LOIN

  ! AANPASSING

       IND      1 2             L=.15              ! BONDING INGANG
       CAP      2 0             C=.075             ! KAP. PAD EN TQCAP900
       TQCAP    2 3             TYPE=1 C=900
       IND      3 4             L=.06              ! INDUK. TQCAP900 EN SOURCE
       TQFET    7 8 4           TYPE=2 W=35 N=4 XIDS=1 VDS=2 STAT=1
       IND      4 5             L=.025             ! INDUK. SOURCE
       L1600    5 6
       MLIN     6 7             W=14 L=125         ! L1600 GATE VERBINDING


  ! VERBINDINGEN

       MLIN     6 17            W=14 L=150         ! L1600 BIAS-FET VERB.
       MLIN     17 15           W=14 L=200         ! BIAS-FET TQCAP2500 VERB.
       CAP      15 0            C=.011             ! KAP. MEETPAD
       IND      15 16           L=.025             ! INDUK. TQCAP2500
       TQCAP    16 99           TYPE=1 C=2500

  ! BIAS FET

       TQFET    18 17 19        TYPE=2 W=35 N=4 XIDS=1 VDS=2 STAT=1
       IND      19 21           L=.05              ! INDUK. SOURCE
       RES      21 18           R=2.5
       CAP      18 0            C=.11              ! KAP. 2*PAD
       IND      18 20           L=.2               ! BONDING NAAR -5V


  ! BIAS AANSLUITING

       MLIN     8 9             W=14 L=240         ! BIAS VERBINDING
       L900     9 10
       MLIN     10 11           W=14 L=180         ! L900 R50 VERBINDING
       TQRES    11 12           TYPE=1 R=50 W=40 H=7
       IND      12 91           L=.05              ! BONDING DC INSTELLING
       CAP      11 0            C=.030             ! KAP. INSTELWEERST.
       MLIN     11 13           W=14 L=250         ! VERB. NAAR MEETPUNT
```

MIXERDEF.CKT

```
        CAP      13 0              C=.011            ! KAP BONDPAD
        CAP      12 0              C=.015          ! KAP. BNDPAD+AANSLT.
        MLIN     9 14              W=14 L=300      ! VERBINDING NAAR MIX


DEF5P   1 14 20 99 91    LOIN


! RFIN

  ! AANPASSING

        IND      25 26             L=.15           ! INGANGS BONDING
        CAP      26 0              C=.1            ! KAP. PAD EN TQCAP2500
        TQCAP    26 27             TYPE=1 C=2500
        IND      27 28             L=.025          ! INDUK. TQCAP2500
        IND      28 29             L=.05           ! SOURCE INDUKTIE
        TQFET    30 31 29          TYPE=2 W=35 N=4 XIDS=1 VDS=2 STAT=1
        L1400    28 32
        MLIN     32 30             W=14 L=140      ! L1400 GATE VERBINDING

  ! VERBINDINGEN

        MLIN     32 33             W=14 L=200      ! L1400 TQCAP2500 VERB.
        IND      33 34             L=.025          ! INDUKTIE TQCAP2500
        TQCAP    34 99             TYPE=1 C=2500
        MLIN     32 35             W=14 L=125      ! L1400 PAD VERBINDING
        CAP      35 0              C=.11           ! KAP 2*PAD
        IND      35 20             L=.2            ! BONDING NAAR -5V


  ! BIAS FET

        TQFET    31 37 36          TYPE=2 W=35 N=4 XIDS=1 VDS=2 STAT=1
        IND      36 38             L=.05           ! SOURCE INDUKTIE
        RES      38 31             R=2.5
        CAP      37 0              C=.022          ! KAP MEETPUNT EN AANSL.
        TQRES    37 97             TYPE=1 R=50 W=40 H=7


  ! VERSTERKERTRAP

        MLIN     31 39             W=14 L=225      ! VERB. NAAR SERIESPOEL
        L500     39 40
        MLIN     40 41             W=14 L=160      ! VERB. NAAR VERSTERKERTRAP
        TQFET    41 42 43          TYPE=2 W=50 N=4 XIDS=.33 VDS=2.1 STAT=1
        IND      42 44             L=.07           ! DRAIN INDUKTIE

  ! BIAS VERSTERKERTRAP

        IND      43 45             L=.07           ! SOURCE INDUKTIE
        TQCAP    45 97             TYPE=1 C=2500
        IND      45 46             L=.03           ! VERBINDING NAAR WEERSTAND
        IND      46 47             L=.025          ! INDUKTIE WEERSTAND
        TQRES    47 48             TYPE=1 R=280 W=20 H=7
```

MIXERDEF.CKT

```
        IND     48 33           L=.025          ! INDUKTIE WEERSTAND
        IND     46 49           L=.03           ! AANSL. MEETPUNT
        CAP     49 0            C=.011          ! KAP BONDPAD 50U

DEF5P   25 44 20 99 97          RFIN


! MIX

        TQFET   14 51 44        TYPE=2 W=50 N=4 XIDS=.17 VDS=2 STAT=1
        IND     50 44           L=.07           ! SOURCE INDUKTIE
        L1000   50 93
        MLIN    51 53           W=14 L=180      ! VERBINDING NAAR IF

DEF4P   14 53 44 93     MIX


! IF

  ! EERSTE FILTER VOOR TWEEDE HARMONISCHE

        MLIN    53 153          W=14 L=90       ! VERB. NAAR L500
        L500    153 154
        MLIN    154 155         W=21 L=150      ! VERB. NAAR PADKAPACITEIT
        CAP     155 0           C=.065          ! KAP. PADS

  ! WEERSTAND 500 OHM

        IND     53 55           L=.04           ! INDUKTIE WEERSTAND
        TQRES   55 56           TYPE=1 R=250 W=20 H=7
        IND     56 57           L=.04           ! INDUKTIE WEERSTAND
        TQRES   57 58           TYPE=1 R=250 W=20 H=7
        IND     58 59           L=.04           ! INDUKTIE WEERSTAND
        CAP     59 0            C=.045          ! KAP. VAN PAD
        IND     59 60           L=.2            ! VERBINDING NAAR +5V
        CAP     60 0            C=100

  ! BUFFERTRAP

        MLIN    53 61           W=14 L=180      ! VERBINDING NAAR GATE FET
        TQFET   61 62 63        TYPE=2 W=25 N=6 XIDS=.66 VDS=2.5 STAT=1
        IND     62 59           L=.06           ! DRAIN INDUKTIE
        TQFET   96 63 96        TYPE=2 W=50 N=2 XIDS=1 VDS=2.5 STAT=1

  ! TWEEDE FILTER VOOR LO

        TQCAP   63 64           TYPE=1 C=500
        L300    64 96

  ! VERBINDING NAAR BUITEN

        CAP     63 0            C=.11           ! KAP 2* PAD
```

MIXERDEF.CKT

```
        IND     63 65           L=.2            ! BONDING NAAR BUITEN

DEF3P   53 65 96     IF



        MLIN    99 98   W=56 L=300
        MLIN    98 97   W=49 L=125
        MLIN    97 96   W=49 L=350
        MLIN    96 93   W=49 L=900
        MLIN    93 92   W=49 L=210
        MLIN    98 92   W=49 L=250
        MLIN    92 91   W=49 L=220
        IND     91 0    L=.15
        IND     96 0    L=.15
        CAP     99 0    C=.1
        CAP     96 0    C=.2
        CAP     91 0    C=.2

DEF5P   99 97 96 93 91       AARDE


! STROOMMETER

        CCCS    500 510 501 0   M=-1 A=0 R1=0 R2=0 F=0 T=0
        DEF3P   500 501 510     STR

! SPANNIGSMETER

        VCVS    600 610 0 0     M=-1 A=0 R1=0 R2=0 F=0 T=0
        DEF2P   600 610         SPN


! SPANNING METING VOOR ZOWEL LOTRAP ALS RFTRAP


        LOIN    1 14 20 99 91
        RFIN    25 44 20 99 97
        CAP     20 0            C=100
        MIX     14 53 44 93
        IF      53 65 96
        MATCH   65
        AARDE   99 97 96 93 91

        SPN     14 614
        SPN     44 644

        DEF4P   1 614 25 644    LORFSPN

! STROOM METING VOOR ZOWEL LOTRAP ALS RFTRAP


        LOIN    1 14 20 99 91
```

MIXERDEF.CKT

```
        AARDE   99 97 96 93 91

        STR     53 530 553

        DEF2P   1 553           IFSTRIN

! STROOM METING UITGANG IFTRAP

        LOIN    1 14 20 99 91
        RFIN    25 44 20 99 97
        MATCH   25
        CAP     20 0            C=100
        MIX     14 53 44 93
        IF      53 65 96
        MATCH   650
        AARDE   99 97 96 93 91

        STR     65 650 565

        DEF2P   1 565           IFSTRUIT

! FELMIXER VOOR UITWENDIGE METINGEN

        LOIN    1 14 20 99 91
        RFIN    25 44 20 99 97
        CAP     20 0            C=100
        MIX     14 53 44 93
        IF      53 65 96
        AARDE   99 97 96 93 91

        DEF3P   1 25 65         FELMIXER


PROC

        LORFMAG=LORFSPN*LORFSTR
        LORFANG=LORFSPN/LORFSTR

        IFINMAG=IFSPNIN*IFSTRIN
        IFINANG=IFSPNIN/IFSTRIN

        IFUITMAG=IFSPNUIT*IFSTRUIT
        IFUITANG=IFSPNUIT/IFSTRUIT

        IFMAG=IFUITMAG/IFINMAG
        IFANG=IFUITANG/IFINANG


OUT

        LORFMAG         MAG[S21]
```

MIXERDEF.CKT

```
        RFIN    25 44 20 99 97
        CAP     20 0            C=100
        MIX     140 53 440 93
        IF      53 65 96
        MATCH   65
        AARDE   99 97 96 93 91

        STR     14 140 514
        STR     44 440 544

        DEF4P   1 514 25 544    LORFSTR

! SPANNING METING INGANG IFTRAP

        LOIN    1 14 20 99 91
        RFIN    25 44 20 99 97
        MATCH   25
        CAP     20 0            C=100
        MIX     14 53 44 93
        IF      53 65 96
        MATCH   65
        AARDE   99 97 96 93 91

        SPN     53 653

        DEF2P   1 653           IFSPNIN

! SPANNING METING UITGANG IFTRAP

        LOIN    1 14 20 99 91
        RFIN    25 44 20 99 97
        MATCH   25
        CAP     20 0            C=100
        MIX     14 53 44 93
        IF      53 65 96
        MATCH   65
        AARDE   99 97 96 93 91

        SPN     65 665

        DEF2P   1 665           IFSPNUIT

! STROOM METING INGANG IFTRAP

        LOIN    1 14 20 99 91
        RFIN    25 44 20 99 97
        MATCH   25
        CAP     20 0            C=100
        MIX     14 53 44 93
        IF      530 65 96
        MATCH   65
```

MIXERDEF.CKT

```
            LORFANG         ANG[S21]

            LORFMAG         MAG[S43]
            LORFANG         ANG[S43]

            IFMAG           MAG[S21]
            IFANG           ANG[S21]


            FELMIXER        DB[S11] GR1
            FELMIXER        DB[S22] GR1
            FELMIXER        DB[S33] GR3
            FELMIXER        DB[S21] GR1
            FELMIXER        DB[S31] GR1

FREQ

            SWEEP   .001 0.101 .020
            SWEEP   .101 2.001 .2
            SWEEP    8 12 .2
            SWEEP   12 24 .5

GRID
            RANGE   8 12 .5
            GR1     -30 0 5
            RANGE   .001 2.001 .25
            GR3     -40 0 5
```

FREQ-GHZ	MAG[S21] LORFMAG	ANG[S21] LORFANG	MAG[S43] LORFMAG	ANG[S43] LORFANG	MAG[S21] IFMAG	ANG[S21] IFANG	DB[S11] FELMIXER	DB[S22] FELMIXER	DB[S33] FELMIXER	DB[S21] FELMIXER	DB[S31] FELMIXER
0.00100	1.1e-11	-92.413	3.1e-08	0.062	0.365	-9.467	-1.2e-05	-6.8e-05	-2.398	-117.190	-71.794
0.02100	9.0e-08	-97.167	8.4e-07	6.898	1.700	-26.104	-0.004	-0.002	-9.134	-77.589	-38.305
0.04100	6.4e-07	-93.491	1.5e-06	12.240	2.008	-14.509	-0.014	-0.002	-14.027	-71.922	-32.237
0.06100	1.9e-06	-91.659	2.7e-06	15.958	2.090	-8.737	-0.027	-0.003	-17.015	-68.886	-29.132
0.08100	3.9e-06	-90.469	4.5e-06	19.417	2.121	-5.199	-0.042	-0.005	-19.032	-66.965	-27.212
0.10100	6.5e-06	-89.557	7.0e-06	22.843	2.134	-2.675	-0.057	-0.007	-20.476	-65.664	-25.941
0.30100	3.3e-05	-83.494	2.1e-04	48.403	2.115	10.340	-0.122	-0.048	-25.604	-62.228	-23.493
0.50100	4.0e-05	-76.998	0.003	59.598	2.036	19.213	-0.116	-0.131	-28.267	-61.987	-24.892
0.70100	6.7e-05	-69.863	0.019	64.901	1.932	26.878	-0.094	-0.262	-31.978	-62.082	-24.454
0.90100	2.3e-04	-66.938	0.081	67.504	1.811	33.615	-0.066	-0.453	-34.858	-62.044	-20.549
1.10100	7.6e-04	-64.363	0.239	68.649	1.685	39.512	-0.041	-0.731	-30.512	-61.159	-16.575
1.30100	0.002	-61.481	0.530	68.916	1.561	44.651	-0.028	-1.122	-25.866	-58.075	-13.396
1.50100	0.004	-58.611	0.941	68.614	1.445	49.128	-0.039	-1.637	-22.508	-53.083	-10.878
1.70100	0.008	-55.948	1.406	67.919	1.337	53.035	-0.090	-2.265	-19.974	-47.838	-8.853
1.90100	0.015	-53.587	1.849	66.936	1.238	56.458	-0.198	-2.980	-17.968	-43.001	-7.206
2.00100	0.019	-52.531	2.045	66.358	1.192	58.012	-0.280	-3.363	-17.108	-40.754	-6.500
8.00000	0.531	-47.076	2.080	45.472	0.084	84.053	-19.124	-18.848	-1.419	-22.970	-12.818
8.20000	0.568	-48.985	2.107	45.808	0.072	83.809	-19.532	-19.378	-1.275	-22.634	-13.471
8.40000	0.608	-50.984	2.143	46.161	0.062	83.512	-19.911	-19.897	-1.148	-22.285	-14.137
8.60000	0.653	-53.057	2.189	46.509	0.053	83.165	-20.263	-20.400	-1.037	-21.928	-14.806
8.80000	0.703	-55.182	2.243	46.829	0.045	82.770	-20.592	-20.878	-0.942	-21.569	-15.460
9.00000	0.758	-57.339	2.307	47.096	0.039	82.332	-20.902	-21.320	-0.865	-21.212	-16.073
9.20000	0.818	-59.507	2.380	47.289	0.034	81.854	-21.200	-21.717	-0.804	-20.861	-16.608
9.40000	0.883	-61.665	2.460	47.384	0.031	81.341	-21.494	-22.059	-0.761	-20.522	-17.021
9.60000	0.953	-63.793	2.547	47.362	0.029	80.799	-21.792	-22.338	-0.736	-20.200	-17.270
9.80000	1.027	-65.875	2.638	47.207	0.029	80.234	-22.109	-22.555	-0.730	-19.900	-17.329
10.0000	1.105	-67.893	2.732	46.903	0.029	79.653	-22.458	-22.713	-0.741	-19.627	-17.196
10.2000	1.184	-69.837	2.825	46.443	0.032	79.061	-22.858	-22.822	-0.771	-19.386	-16.900
10.4000	1.263	-71.695	2.915	45.819	0.035	78.464	-23.329	-22.898	-0.818	-19.181	-16.488
10.6000	1.340	-73.460	3.000	45.029	0.039	77.870	-23.899	-22.957	-0.884	-19.016	-16.009
10.8000	1.413	-75.127	3.076	44.075	0.044	77.284	-24.603	-23.013	-0.968	-18.895	-15.507
11.0000	1.481	-76.692	3.140	42.960	0.050	76.711	-25.487	-23.077	-1.069	-18.820	-15.014
11.2000	1.541	-78.155	3.192	41.689	0.056	76.156	-26.621	-23.150	-1.187	-18.791	-14.552
11.4000	1.593	-79.515	3.229	40.270	0.063	75.621	-28.119	-23.222	-1.322	-18.808	-14.133
11.6000	1.636	-80.773	3.253	38.711	0.071	75.110	-30.191	-23.264	-1.472	-18.867	-13.764
11.8000	1.669	-81.931	3.264	37.017	0.078	74.622	-33.307	-23.233	-1.638	-18.964	-13.446
12.0000	1.694	-82.992	3.263	35.194	0.086	74.160	-38.938	-23.066	-1.819	-19.089	-13.179
12.5000	1.722	-85.235	3.225	30.072	0.103	73.095	-33.662	-21.676	-2.332	-19.412	-12.708
13.0000	1.717	-86.928	3.166	24.001	0.118	72.104	-24.131	-18.850	-2.925	-19.334	-12.469
13.5000	1.695	-88.102	3.127	16.361	0.127	71.048	-18.481	-15.277	-3.578	-18.013	-12.409
14.0000	1.646	-88.796	3.163	5.356	0.131	69.671	-13.844	-11.427	-4.272	-14.958	-12.538
14.5000	1.460	-89.233	3.433	-12.821	0.130	67.471	-9.527	-7.472	-5.056	-10.732	-13.066
15.0000	0.790	-91.878	4.167	-36.424	0.156	63.488	-6.082	-4.276	-6.320	-6.821	-14.616
15.5000	0.119	-155.896	3.929	-44.076	1.188	72.604	-5.700	-4.200	-8.040	-5.858	-15.483
16.0000	0.159	-145.532	3.031	-32.786	1.199	124.069	-7.643	-6.668	-8.620	-7.307	-14.211
16.5000	0.316	-112.129	2.740	-20.672	0.633	97.860	-9.617	-9.598	-8.573	-9.004	-13.252
17.0000	0.451	-102.450	2.710	-13.602	0.480	89.747	-11.008	-12.687	-8.398	-10.434	-12.614
17.5000	0.544	-97.429	2.699	-9.522	0.419	85.840	-11.777	-16.336	-8.198	-11.596	-12.152
18.0000	0.606	-93.760	2.615	-6.575	0.387	82.914	-12.001	-21.128	-7.994	-12.481	-11.881
18.5000	0.649	-90.848	2.421	-3.762	0.364	79.336	-11.794	-24.477	-7.730	-13.014	-11.894
19.0000	0.681	-88.802	2.131	-0.514	0.341	72.674	-11.242	-20.651	-7.291	-13.128	-12.324
19.5000	0.718	87.911	1.799	3.569	0.309	55.989	-10.342	-16.928	-6.591	-12.854	-13.331
20.0000	0.786	-88.399	1.492	8.855	0.207	12.656	-8.966	-14.415	-5.629	-12.273	-14.864
20.5000	0.948	-90.229	1.279	15.696	0.108	-29.077	-6.796	-12.529	-4.439	-11.349	-13.837
21.0000	1.413	-92.402	1.271	23.518	0.189	-43.806	-3.130	-10.714	-3.079	-9.576	-5.938
21.5000	1.689	-88.407	1.214	21.061	0.427	-47.895	0.676	-9.961	-5.329	-7.008	2.163
22.0000	0.234	-42.279	0.389	2.595	0.90[illegible]	-47.389	-4.495	-12.471	-15.061	-9.543	-0.330
22.5000	0.112	-3.389	0.212	4.366	2.68[illegible]	-42.975	-8.952	-12.059	-9.434	-10.669	-3.783
23.0000	0.067	3.910	0.134	8.472	24.999	108.077	-11.523	-11.396	-8.339	-11.030	-6.468
23.5000	0.039	14.045	0.082	12.618	2.921	140.888	-13.607	-10.745	-8.347	-11.309	-8.875
24.0000	0.024	16.224	0.043	25.821	1.511	147.486	-16.313	-10.071	-8.673	-11.615	-10.948

Appendix C

RESULTS OF STABILITY SIMULATIONS

FREQ-GHZ	K KRFIF	B1 KRFIF	MAG[SB1] KRFIF	ANG[SB1] KRFIF	RAD[SB1] KRFIF	PAR[SB1] KRFIF	MAG[SB2] KRFIP	ANG[SB2] KRFIF	RAD[SB2] KRFIF	PAR[SB2] KRFIF
0.00100	999.900	0.849	1.000	0.094	2.2e-10	1.000	1.320	5.703	1.0e-05	1.000
0.02100	999.900	1.756	1.000	1.922	2.9e-09	1.000	2.862	71.038	5.3e-05	1.000
0.04100	999.900	1.920	1.000	3.750	1.6e-09	1.000	5.027	90.872	7.0e-05	1.000
0.06100	999.900	1.959	1.000	5.577	9.2e-10	1.000	7.092	102.566	5.7e-05	1.000
0.08100	999.900	1.974	1.001	7.404	4.6e-10	1.000	8.946	111.444	3.2e-05	1.000
0.10100	999.900	1.981	1.001	9.230	1.4e-10	1.000	10.564	118.762	1.0e-05	1.000
0.30100	3.9e+05	1.984	1.006	27.391	1.4e-08	1.000	19.064	155.195	4.6e-04	1.000
0.50100	8.8e+04	1.967	1.015	45.240	1.7e-07	1.000	25.902	165.526	0.004	1.000
0.70100	3.9e+04	1.940	1.031	62.638	8.0e-07	1.000	39.704	159.329	0.020	1.000
0.90100	2.9e+04	1.900	1.054	79.502	1.9e-06	1.000	55.322	118.351	0.052	1.000
1.10100	6.1e+03	1.843	1.088	95.744	1.5e-05	1.000	33.563	79.096	0.092	1.000
1.30100	1.8e+03	1.768	1.138	111.203	8.0e-05	1.000	19.648	69.684	0.105	1.000
1.50100	797.823	1.677	1.207	125.648	2.9e-04	1.000	13.327	69.253	0.111	1.000
1.70100	420.159	1.578	1.298	138.866	8.1e-04	1.000	9.933	71.589	0.116	1.000
1.90100	247.289	1.480	1.409	150.760	0.002	1.000	7.862	74.960	0.123	1.000
2.00100	194.772	1.433	1.473	156.213	0.003	1.000	7.110	76.825	0.127	1.000
8.00000	17.517	0.282	9.144	-117.888	2.218	1.000	1.178	173.037	0.011	1.000
8.20000	17.974	0.257	9.730	-119.084	2.440	1.000	1.158	176.215	0.009	1.000
8.40000	18.575	0.235	10.416	-120.597	2.698	1.000	1.141	179.400	0.008	1.000
8.60000	19.144	0.214	11.277	-122.568	3.052	1.000	1.127	-177.412	0.007	1.000
8.80000	19.215	0.196	12.456	-125.247	3.662	1.000	1.115	-174.222	0.006	1.000
9.00000	18.143	0.182	14.272	-129.055	4.919	1.000	1.105	-171.032	0.006	1.000
9.20000	15.833	0.170	17.535	-134.638	7.771	1.000	1.097	-167.847	0.006	1.000
9.40000	13.075	0.161	24.942	-142.801	15.069	1.000	1.092	-164.669	0.007	1.000
9.60000	10.651	0.156	51.867	-154.015	42.289	1.000	1.089	-161.504	0.009	1.000
9.80000	8.816	0.155	497.013	12.724	505.907	-1.000	1.088	-158.356	0.010	1.000
10.0000	7.515	0.157	56.765	0.204	64.767	-1.000	1.090	-155.233	0.012	1.000
10.2000	6.615	0.162	41.102	-9.160	48.234	-1.000	1.094	-152.140	0.015	1.000
10.4000	5.997	0.171	42.300	-14.944	48.708	-1.000	1.100	-149.083	0.017	1.000
10.6000	5.572	0.184	54.540	-17.926	60.387	-1.000	1.108	-146.070	0.020	1.000
10.8000	5.276	0.200	95.384	-19.041	100.800	-1.000	1.119	-143.106	0.024	1.000
11.0000	5.063	0.218	759.036	-19.015	764.116	-1.000	1.132	-140.198	0.028	1.000
11.2000	4.902	0.239	117.512	161.655	112.708	1.000	1.148	-137.350	0.032	1.000
11.4000	4.769	0.263	53.465	162.658	48.898	1.000	1.165	-134.568	0.037	1.000
11.6000	4.651	0.288	34.255	163.811	29.904	1.000	1.186	-131.854	0.043	1.000
11.8000	4.535	0.316	24.970	165.020	20.824	1.000	1.208	-129.213	0.050	1.000
12.0000	4.416	0.345	19.448	166.250	15.502	1.000	1.234	-126.648	0.059	1.000
12.5000	4.072	0.421	11.975	169.494	8.536	1.000	1.307	-120.573	0.086	1.000
13.0000	3.637	0.503	8.045	173.492	5.135	1.000	1.398	-114.959	0.129	1.000
13.5000	3.088	0.588	5.545	179.246	3.180	1.000	1.504	-109.603	0.198	1.000
14.0000	2.417	0.686	3.794	-171.447	1.969	1.000	1.635	-103.683	0.324	1.000
14.5000	1.671	0.824	2.559	-154.775	1.217	1.000	1.852	-94.321	0.614	1.000
15.0000	1.144	1.035	1.876	-124.901	0.813	1.000	2.794	-75.464	1.705	1.000
15.5000	1.564	1.109	1.911	-87.667	0.694	1.000	5.755	-72.728	4.315	1.000
16.0000	3.244	1.013	2.503	-60.059	0.730	1.000	3.624	-98.084	1.516	1.000
16.5000	6.180	0.939	3.430	-40.662	0.817	1.000	2.948	-109.203	0.594	1.000
17.0000	10.953	0.894	4.797	-22.974	0.963	1.000	2.719	-113.251	0.288	1.000
17.5000	18.629	0.865	7.224	-1.802	1.327	1.000	2.600	-114.964	0.154	1.000
18.0000	29.636	0.847	12.564	32.530	2.538	1.000	2.519	-115.919	0.090	1.000
18.5000	43.187	0.834	17.241	100.933	3.304	1.000	2.436	-116.797	0.057	1.000
19.0000	61.599	0.821	10.577	156.145	0.893	1.000	2.313	-117.528	0.035	1.000
19.5000	91.518	0.797	6.929	-176.065	0.256	1.000	2.134	-117.220	0.019	1.000
20.0000	122.242	0.753	5.206	-156.963	0.107	1.000	1.910	-114.516	0.011	1.000
20.5000	86.218	0.677	4.177	-140.874	0.095	1.000	1.665	-107.540	0.010	1.000
21.0000	20.323	0.554	3.338	-122.176	0.248	1.000	1.421	-90.583	0.025	1.000
21.5000	5.297	0.764	3.689	-87.028	1.080	1.000	1.916	-40.100	0.246	1.000
22.0000	11.682	1.024	4.231	-88.700	0.702	1.000	5.734	-106.928	1.293	1.000
22.5000	18.379	0.944	3.917	-84.462	0.386	1.000	2.927	-108.462	0.205	1.000
23.0000	23.342	0.918	3.646	-76.447	0.262	1.000	2.590	-100.375	0.122	1.000
23.5000	26.179	0.928	3.397	-67.086	0.201	1.000	2.594	-94.535	0.109	1.000
24.0000	26.148	0.952	3.150	-56.697	0.170	1.000	2.692	-91.712	0.119	1.000

Appendix C

FREQ-GHZ	K KLORF	B1 KLORF	MAG[SB1] KLORF	ANG[SB1] KLORF	RAD[SB1] KLORF	PAR[SB1] KLORF	MAG[SB2] KLORF	ANG[SB2] KLORF	RAD[SB2] KLORF	PAR[SB2] KLORF
0.00100	999.900	3.1e-05	1.001	0.035	1.3e-07	1.000	0.996	0.092	7.5e-07	1.000
0.02100	8.589	7.7e-04	1.000	0.732	4.9e-05	1.000	1.000	1.922	2.1e-05	1.000
0.04100	13.242	0.001	1.002	1.405	1.3e-04	1.000	1.000	3.749	2.2e-05	1.000
0.06100	18.589	0.002	1.003	2.046	1.8e-04	1.000	1.000	5.576	2.2e-05	1.000
0.08100	25.869	0.002	1.005	2.655	1.9e-04	1.000	1.001	7.403	2.2e-05	1.000
0.10100	35.234	0.003	1.007	3.236	1.9e-04	1.000	1.001	9.229	2.3e-05	1.000
0.30100	228.282	0.022	1.014	8.572	6.2e-05	1.000	1.006	27.390	2.4e-05	1.000
0.50100	515.250	0.059	1.013	13.978	2.6e-05	1.000	1.015	45.239	3.0e-05	1.000
0.70100	640.153	0.116	1.011	19.584	1.7e-05	1.000	1.031	62.636	4.8e-05	1.000
0.90100	452.468	0.197	1.008	25.418	1.7e-05	1.000	1.053	79.498	1.2e-04	1.000
1.10100	208.454	0.308	1.005	31.523	2.3e-05	1.000	1.088	95.728	4.4e-04	1.000
1.30100	79.915	0.454	1.003	37.950	4.0e-05	1.000	1.137	111.130	0.002	1.000
1.50100	51.873	0.625	1.004	44.745	8.6e-05	1.000	1.205	125.476	0.004	1.000
1.70100	54.605	0.804	1.010	51.948	1.9e-04	1.000	1.294	138.652	0.006	1.000
1.90100	58.371	0.971	1.023	59.582	4.0e-04	1.000	1.404	150.524	0.008	1.000
2.00100	58.625	1.045	1.033	63.563	5.6e-04	1.000	1.466	155.967	0.010	1.000
8.00000	126.245	0.999	9.087	-147.881	0.323	1.000	8.800	-106.072	0.302	1.000
8.20000	124.042	0.999	9.526	-142.747	0.361	1.000	9.357	-106.637	0.348	1.000
8.40000	121.750	1.000	9.954	-137.313	0.402	1.000	9.938	-107.538	0.401	1.000
8.60000	119.405	1.000	10.369	-131.571	0.445	1.000	10.536	-108.792	0.460	1.000
8.80000	116.975	1.000	10.772	-125.519	0.491	1.000	11.137	-110.407	0.525	1.000
9.00000	114.345	1.001	11.167	-119.160	0.540	1.000	11.725	-112.376	0.595	1.000
9.20000	111.305	1.001	11.561	-112.503	0.594	1.000	12.280	-114.668	0.671	1.000
9.40000	107.569	1.001	11.963	-105.565	0.659	1.000	12.781	-117.228	0.752	1.000
9.60000	102.833	1.001	12.390	-98.362	0.739	1.000	13.209	-119.977	0.840	1.000
9.80000	96.908	1.000	12.863	-90.917	0.845	1.000	13.554	-122.820	0.938	1.000
10.0000	89.859	1.000	13.409	-83.255	0.989	1.000	13.817	-125.663	1.051	1.000
10.2000	82.052	1.000	14.070	-75.401	1.192	1.000	14.012	-128.435	1.182	1.000
10.4000	74.046	0.999	14.903	-67.381	1.478	1.000	14.161	-131.102	1.335	1.000
10.6000	66.399	0.999	15.994	-59.216	1.892	1.000	14.290	-133.681	1.513	1.000
10.8000	59.508	0.998	17.477	-50.923	2.505	1.000	14.426	-136.248	1.715	1.000
11.0000	53.573	0.998	19.590	-42.505	3.461	1.000	14.584	-138.928	1.940	1.000
11.2000	48.631	0.997	22.798	-33.937	5.069	1.000	14.766	-141.892	2.182	1.000
11.4000	44.623	0.997	28.187	-25.135	8.148	1.000	14.952	-145.338	2.428	1.000
11.6000	41.439	0.996	39.157	-15.850	15.565	1.000	15.086	-149.458	2.649	1.000
11.8000	38.958	0.996	76.322	-5.269	46.726	1.000	15.075	-154.382	2.803	1.000
12.0000	37.052	0.995	154.382	-168.980	195.815	-1.000	14.798	-160.093	2.833	1.000
12.5000	33.927	0.993	83.069	-174.547	55.798	1.000	12.475	-175.707	2.207	1.000
13.0000	30.981	0.991	16.690	-149.804	4.195	1.000	8.855	173.057	1.225	1.000
13.5000	24.662	0.985	8.385	-128.072	1.367	1.000	5.802	170.244	0.654	1.000
14.0000	13.669	0.969	4.837	-103.768	0.796	1.000	3.690	176.148	0.454	1.000
14.5000	4.012	0.928	2.888	-70.810	0.829	1.000	2.312	-166.533	0.509	1.000
15.0000	0.734	0.853	2.051	-19.373	1.202	1.000	1.650	-130.499	0.770	1.000
15.5000	0.455	0.850	2.474	35.669	1.853	1.000	1.925	-87.315	1.251	1.000
16.0000	0.870	0.917	3.742	72.737	2.839	1.000	3.048	-59.867	2.138	1.000
16.5000	1.347	0.961	5.552	100.325	4.278	1.000	5.523	-42.376	4.250	1.000
17.0000	1.754	0.987	7.877	125.022	6.254	1.000	17.987	-28.208	16.290	1.000
17.5000	2.081	1.004	10.414	149.457	8.492	1.000	11.793	165.568	14.014	-1.000
18.0000	2.329	1.014	11.942	174.485	9.797	1.000	3.146	-178.903	6.114	-1.000
18.5000	2.481	1.019	11.103	-160.449	8.851	1.000	0.701	-148.018	4.858	-1.000
19.0000	2.512	1.021	8.663	-137.063	6.452	1.000	1.373	8.964	5.195	-1.000
19.5000	2.416	1.026	6.221	-116.878	4.182	1.000	4.528	30.399	7.449	-1.000
20.0000	2.180	1.044	4.307	-99.925	2.542	1.000	16.236	46.782	18.532	-1.000
20.5000	1.716	1.103	2.832	-84.347	1.441	1.000	43.324	-116.108	41.630	1.000
21.0000	0.772	1.340	1.648	-63.478	0.749	1.000	14.748	-93.357	13.962	1.000
21.5000	-0.215	2.011	1.004	-9.662	0.446	1.000	10.932	-66.806	11.103	1.000
22.0000	1.500	1.294	1.733	40.946	0.563	1.000	5.151	-82.477	3.770	1.000
22.5000	3.390	1.064	2.886	54.096	0.948	1.000	4.252	-85.815	1.955	1.000
23.0000	4.498	0.996	3.920	61.471	1.384	1.000	3.859	-79.176	1.343	1.000
23.5000	5.251	0.957	5.156	69.744	2.040	1.000	3.575	-70.056	1.022	1.000
24.0000	5.637	0.920	8.106	77.998	4.185	1.000	3.335	-59.366	0.836	1.000

FREQ-GHZ	K KLOIF	B1 KLOIF	MAG[SB1] KLOIF	ANG[SB1] KLOIF	RAD[SB1] KLOIF	PAR[SB1] KLOIF	MAG[SB2] KLOIF	ANG[SB2] KLOIF	RAD[SB2] KLOIF	PAR[SB2] KLOIF
0.00100	999.900	0.849	1.000	0.035	4.1e-11	1.000	1.302	5.711	1.1e-05	1.000
0.02100	999.900	1.755	1.000	0.732	6.4e-09	1.000	2.862	71.037	5.2e-05	1.000
0.04100	5.8e+04	1.918	1.002	1.408	2.7e-08	1.000	5.028	90.869	2.1e-04	1.000
0.06100	6.1e+04	1.954	1.003	2.053	5.2e-08	1.000	7.092	102.563	4.0e-04	1.000
0.08100	7.0e+04	1.965	1.005	2.664	7.0e-08	1.000	8.945	111.441	5.6e-04	1.000
0.10100	8.9e+04	1.969	1.007	3.246	7.4e-08	1.000	10.563	118.759	6.2e-04	1.000
0.30100	1.5e+04	1.967	1.014	8.575	9.3e-07	1.000	19.070	155.226	0.012	1.000
0.50100	3.9e+03	1.971	1.013	13.979	3.5e-06	1.000	25.916	165.720	0.086	1.000
0.70100	1.1e+03	1.977	1.011	19.585	9.7e-06	1.000	39.494	160.293	0.689	1.000
0.90100	238.485	1.984	1.008	25.419	3.2e-05	1.000	55.588	124.952	6.391	1.000
1.10100	49.809	1.989	1.005	31.524	9.5e-05	1.000	45.594	98.232	17.710	1.000
1.30100	13.698	1.988	1.003	37.952	2.3e-04	1.000	2.1e+03	-64.423	2.1e+03	-1.000
1.50100	8.892	1.980	1.005	44.750	5.1e-04	1.000	48.409	-62.046	58.101	-1.000
1.70100	10.374	1.960	1.010	51.958	0.001	1.000	33.222	95.152	24.416	1.000
1.90100	12.506	1.924	1.023	59.600	0.002	1.000	13.111	86.110	5.585	1.000
2.00100	13.366	1.899	1.033	63.585	0.003	1.000	10.563	84.829	3.641	1.000
8.00000	11.547	0.282	10.034	-166.142	3.717	1.000	1.178	173.008	0.017	1.000
8.20000	10.567	0.257	11.046	-164.125	4.687	1.000	1.158	176.182	0.016	1.000
8.40000	9.704	0.234	12.424	-162.221	6.029	1.000	1.142	179.362	0.016	1.000
8.60000	8.948	0.214	14.495	-160.471	8.057	1.000	1.127	-177.451	0.015	1.000
8.80000	8.292	0.196	18.084	-158.935	11.578	1.000	1.115	-174.261	0.015	1.000
9.00000	7.724	0.181	26.045	-157.706	19.423	1.000	1.105	-171.069	0.014	1.000
9.20000	7.229	0.169	59.620	-156.942	52.819	1.000	1.098	-167.879	0.014	1.000
9.40000	6.792	0.161	83.307	23.070	90.369	-1.000	1.093	-164.694	0.014	1.000
9.60000	6.395	0.156	19.158	21.763	26.568	-1.000	1.090	-161.520	0.015	1.000
9.80000	6.032	0.154	8.947	17.914	16.776	-1.000	1.089	-158.361	0.015	1.000
10.0000	5.702	0.156	4.892	8.761	13.147	-1.000	1.090	-155.222	0.017	1.000
10.2000	5.411	0.161	3.008	-10.867	11.521	-1.000	1.094	-152.112	0.018	1.000
10.4000	5.169	0.170	2.505	-40.227	10.825	-1.000	1.101	-149.036	0.020	1.000
10.6000	4.977	0.182	2.921	-61.837	10.660	-1.000	1.109	-146.001	0.023	1.000
10.8000	4.832	0.198	3.725	-70.731	10.851	-1.000	1.120	-143.015	0.026	1.000
11.0000	4.728	0.216	4.703	-72.224	11.321	-1.000	1.133	-140.083	0.030	1.000
11.2000	4.655	0.237	5.838	-69.709	12.054	-1.000	1.149	-137.213	0.034	1.000
11.4000	4.604	0.260	7.190	-64.761	13.083	-1.000	1.167	-134.410	0.039	1.000
11.6000	4.566	0.285	8.895	-58.166	14.514	-1.000	1.188	-131.680	0.045	1.000
11.8000	4.532	0.312	11.214	-50.381	16.586	-1.000	1.211	-129.029	0.051	1.000
12.0000	4.496	0.340	14.724	-41.721	19.859	-1.000	1.236	-126.463	0.058	1.000
12.5000	4.357	0.415	56.587	-17.702	61.103	-1.000	1.312	-120.463	0.082	1.000
13.0000	4.092	0.493	27.901	-172.168	24.090	1.000	1.404	-115.153	0.117	1.000
13.5000	3.660	0.572	9.872	-145.953	6.821	1.000	1.514	-110.660	0.173	1.000
14.0000	3.066	0.660	5.200	-117.774	2.887	1.000	1.640	-107.083	0.264	1.000
14.5000	2.413	0.781	3.023	-83.413	1.323	1.000	1.789	-104.504	0.420	1.000
15.0000	2.116	0.977	2.008	-35.714	0.624	1.000	2.064	-104.003	0.666	1.000
15.5000	2.809	1.076	1.958	19.163	0.466	1.000	2.618	-108.876	0.898	1.000
16.0000	4.046	1.012	2.478	61.773	0.592	1.000	2.799	-113.104	0.771	1.000
16.5000	5.602	0.954	3.126	94.240	0.735	1.000	2.749	-115.124	0.557	1.000
17.0000	7.216	0.921	3.700	122.581	0.831	1.000	2.682	-116.349	0.417	1.000
17.5000	8.532	0.902	4.094	149.105	0.879	1.000	2.622	-117.071	0.338	1.000
18.0000	9.232	0.890	4.258	174.000	0.885	1.000	2.567	-117.623	0.298	1.000
18.5000	9.387	0.881	4.192	-163.308	0.845	1.000	2.495	-118.325	0.274	1.000
19.0000	9.429	0.868	3.930	-143.202	0.737	1.000	2.372	-118.963	0.242	1.000
19.5000	9.757	0.846	3.519	-125.384	0.567	1.000	2.185	-118.504	0.192	1.000
20.0000	10.251	0.808	3.003	-108.697	0.384	1.000	1.959	-115.409	0.138	1.000
20.5000	6.999	0.752	2.412	-89.998	0.336	1.000	1.740	-107.120	0.143	1.000
21.0000	1.227	0.682	1.876	-53.997	0.779	1.000	1.849	-75.755	0.754	1.000
21.5000	0.349	0.878	4.920	16.324	4.481	1.000	1.194	-121.650	1.089	-1.000
22.0000	0.965	0.985	31.204	34.336	30.238	1.000	0.689	-50.949	1.603	-1.000
22.5000	1.627	0.909	13.164	38.084	11.599	1.000	29.485	-127.453	27.886	1.000
23.0000	2.405	0.882	8.008	47.049	5.896	1.000	3.389	-108.085	1.629	1.000
23.5000	3.508	0.879	7.515	60.011	4.725	1.000	2.888	-98.799	0.925	1.000
24.0000	4.958	0.878	10.050	72.973	6.203	1.000	2.864	-94.318	0.680	1.000

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GAAS MMIC MIXER FOR 8-12GHZ, BASED ON 0.5 μM GATE LENGTH D-MESFETS.
VOLUME 1: DESIGN AND LAYOUT.

11. AUTHOR(S)

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14. SUPPLEMENTARY NOTES

15. ABSTRACT (MAXIMUM 200 WORDS, 1044 POSITIONS)

A DESCRIPTION IS GIVEN OF THE DESIGN OF AN 8-12 GHZ GAAS MMIC (MONOLITHIC MICROWAVE INTEGRATED CIRCUIT) MIXER. THE MIXER CONSISTS OF A DUAL-FET MIXING ELEMENT, ACTIVE INPUT AND OUTPUT MATCHING AND BIAS NETWORKS. THE MIXER IS DESIGNED WITH THE TRIQUINT HA-PROCESS WHICH USES 0.5μM GATE LENGTH DEPLETION MODE MESFET DEVICES.
THE DESIGN GOALS ARE A RETURN LOSS BETTER THAN -15DB FOR THE INPUTS AND OUTPUT AND A CONVERSION GAIN BETTER THAN 0DB. THE COMPLETE CIRCUIT IS BIASED WITH A SYMMETRICAL POWER SUPPLY OF ±5 VOLTS AND HAS AUTOBIASING THROUGH ON-CHIP BIAS NETWORKS. THE ESTIMATED TOTAL POWER CONSUMPTION OF THE CIRCUIT IS 350MW.THE DIMENSIONS OF THE CHIP ARE 1.4X1.4MM.
THIS REPORT IS PART ONE OF TWO REPORTS AND GIVES AN IN-DEPTH DESCRIPTION OF THE CIRCUIT DESIGN. SIMULATION RESULTS AND CHIP LAYOUT ARE PROVIDED. A SECOND REPORT WILL GIVE THE MEASUREMENT RESULTS AS WELL AS AN EVALUATION OF THEM.

16. DESCRIPTORS	IDENTIFIERS
INTEGRATED CIRCUITS	MMIC
X-BAND	
MICROWAVES	
GALLIUM ARSENIDE (GAAS)	

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